Design of Nano Scale Based Logic Gates Using Quantum-dot cellular Automata

Aswathy N[1], Rahul Krishnan[1,2]

[1]Lincoln University College, Malaysia; [2]Sree Buddha College of Engineering India

pdf.aswathy@lincoln.edu.my

Abstract: As complementary metal–oxide–semiconductor (CMOS) technology approaches its fundamental scaling limits, emerging nanotechnologies have gained significant attention as potential alternatives. Among these, Quantum-dot Cellular Automata (QCA) has emerged as a promising model due to its ultra-low power consumption, high device density, and nanoscale operation. This work explores the design and analysis of fundamental QCA logic gates, including AND, NAND, OR, NOR, XOR, and XNOR. The proposed designs are evaluated based on key performance metrics such as cell count, occupied area and latency. Functional verification and performance analysis are carried out using QCADesigner version 2.0.3. Furthermore, the energy efficiency of the implemented logic gates is assessed using the QCADesigner-E tool.

Keywords: Polarization, quantum-dot, logic gates, energy consumption.

Introduction

The increasing demand for superior-performance and energy-efficient system has driven the exploration of technologies beyond conventional silicon-based electronics. The physical scaling constraints and significant power dissipation associated with CMOS technology have necessitated the development of alternative computing paradigms. QCA has emerged as a viable candidate, leveraging quantum-mechanical principles to enable efficient nanoscale computation. High switching speed, enhanced packing density, and decreased energy dissipation are some of the distinctive characteristics that set QCA apart. A cell made up of four quantum dots, each with two electrons that can tunnel between neighbouring dots, is the fundamental building block of QCA. The logical state of the cell is determined by the electrons' positions. Unlike typical CMOS, which uses the passage of electrical current to transport information, QCA technology uses coulombic interactions between adjacent cells [1, 2]. The data is transferred with the help of a four phase clocking scheme. The basic QCA gates available are inverter and majority gate (MG). Inverter provides the inversion of polarized cells. The majority gate has three inputs and it provide the majority of inputs as output [3].

Related work

Since QCA-based digital circuits provide a novel method of data processing and logic operations without depending on traditional transistors, they have attracted a lot of research interest [4,5]. The previous works were done using CMOS logic like double pass transistor logic based clocked CMOS (DPTL-C^{2}MOS) implementation of logic gates [6]. Due to its volatile nature complete cut-off is not possible. So a significant amount of power dissipation occurs in this logic. To reduce the power dissipation, another post CMOS logic called spintronics was explored. In [7], spintronics based hybrid gates was proposed using

logic -in-memory architecture. Another work in [8] uses SHE-assisted spintronics based logic gates were introduced to shrink the power consumption. So the energy dissipation is reduced from CMOS logic. Further reduction in energy is possible with the help of QCA.

Key Contribution

This paper provides the following,

(1) The application of QCA-based logic gates.

(2) A comparison between the suggested gate design and earlier research.

(3) QCADesigner-E Tool energy dissipation estimation.

Method, Experiments and Results

The basic modules for any digital circuits are the basic gates like inverter, AND, OR, NAND, NOR, XOR and XNOR gates. The optimization of these gates using CMOS technology is no longer applicable due to second order effects. So the researchers are trying to optimize the basic gates using new technologies. Hence, the implementation of the logic gates using QCA is discussed in this session. The circuits are optimized in terms of parameters like cell count, area and latency. In QCA, majority and inverter gates were used to build logic gates. The proposed work consists of gates like AND/NAND, OR/NOR, and XOR/XNOR. The truth tables for basic gates are shown in Table 1.

Table1: Basic logic gate truth table

Input values		Output Values		
A input	B input	AND/NAND	OR/NOR	XOR/XNOR
0	0	0/1	0/1	0/1
0	1	0/1	1/0	1/0
1	0	0/1	1/0	1/0
1	1	1/1	1/0	0/1

Gate using QCA AND/NAND

One way to obtain a two-input AND gates from a 3-bit majority gate is to fix one of the input cell polarizations (Pz) = '-1'. Similarly, the NAND gate is made by adding an inverter gate to the AND gate. Assume that A and B are the inputs. NAND and AND are the outputs. The layout and simulation results are displayed in Figures 1 and 2 respectively. The AND/NAND QCA circuit 0.25 clock cycles delay, complexity of nine cells, and an area of 0.01 um^2.

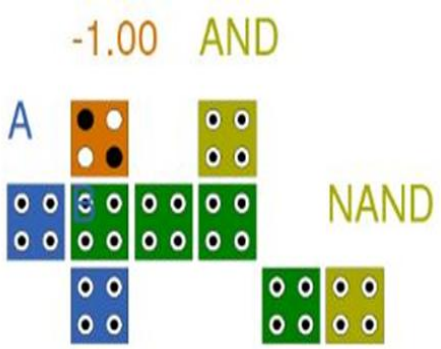

Figure 1. QCA AND/NAND

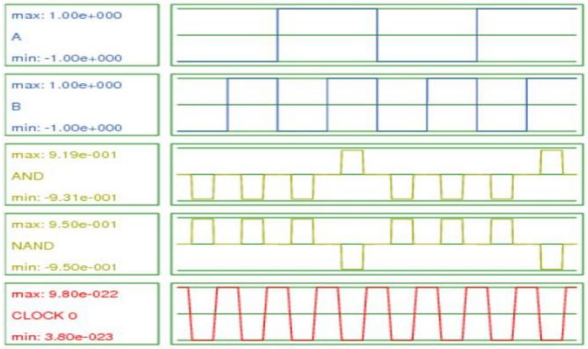

Figure 2. Output of AND/NAND

OR/NOR Gate using QCA

The OR gate can be obtained in QCA by using a majority gate. The OR function can be triggered by setting one of the majority gate's inputs to logic "1". The complementary function is produced by inverting the true form, as shown in Figure 3. Nine cells make up the OR/NOR structure, which has an area of 0.01 um^2 and a delay of one phase clock cycle. The simulation result displayed in Figure 4 confirms the functioning.

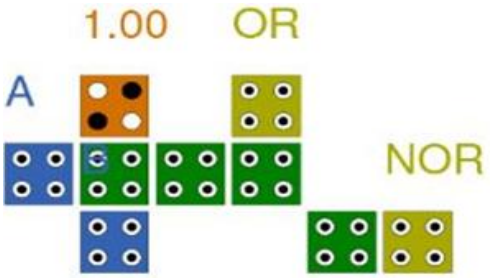

Figure 3. QCA functional layout of OR/NOR gate

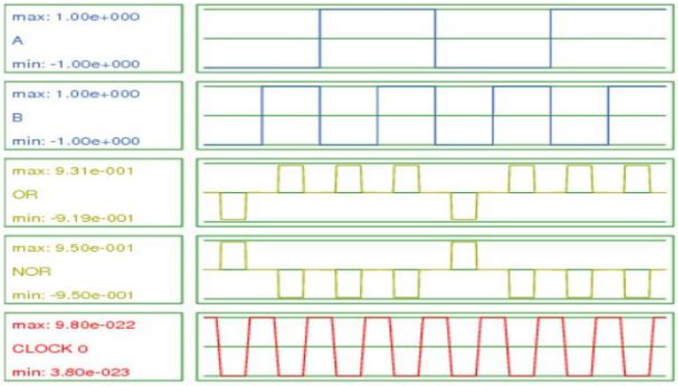

Figure 4. Output of OR/NOR gate

XOR/XNOR Gate using QCA

Majority and inverter gates are also used in the construction of the XOR/XNOR gate. Equation (1) is used to represent the XOR logic.

$$XOR = A \oplus B = MG((MG(A', B, 0), MG(A, B', 0), 1) \quad (1)$$

The XNOR is produced by inverting the XOR value, as shown in Figure 5. In this case, a basic inverter is employed. Figure 6 depicts the output result. The layout consists of 34 cells with a 0.05 um^2 area and a 0.5 clock cycle latency.

Energy Estimation of Logic Gates

The QCADesigner-E [9, 10] tool was used to estimate the energy of logic gates used in QCA technology. The AND/NAND, OR/NOR, and XOR/XNOR gates have respective total energy dissipations of 4.39 meV, 3.97 meV, and 16.1 meV. The coherence vector simulation engine is used to calculate it.

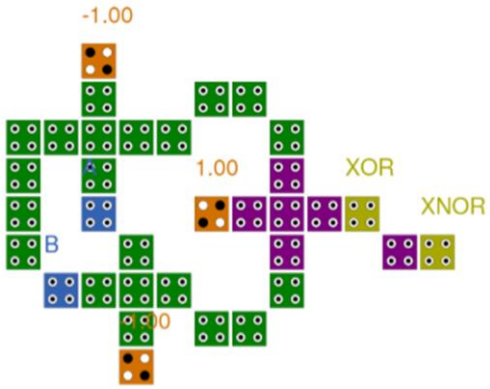

Figure 5. QCA functional layout of XOR/XNOR gate

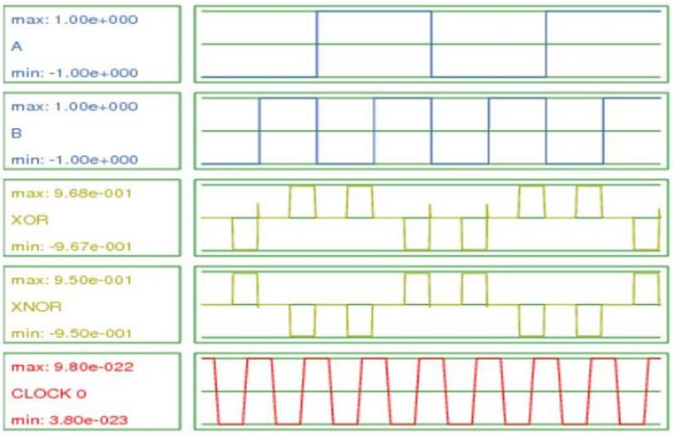

Figure 6. Output of XOR/XNOR gate

Discussions

In the future, when energy efficiency, speed, and density are the primary requirements, a transistor-less nanotechnology called QCA is thought to be the best substitute for CMOS. Table 2 provides the performance metrics taken into account while choosing QCA as the successor of CMOS.

Table 2. Comparison of CMOS, Spintronics and QCA based Logic Gates Performance

Logic gates	CMOS(45nm) [7]			Spintronics [8]			Proposed QCA
	Power (nW)	Delay (ps)	Energy (mev)	Power (nW)	Delay (ps)	Energy (mev)	Energy (mev)
AND/NAND	162	83.9	84260.3	44.5	125.2	34328.2	4.39
OR/NOR	180	80.9	90501.8	47.8	120.2	35576.5	3.97
XOR/XNOR	199	84	104233.1	48.7	152	46187.1	16.1

Conclusion

QCA is the most promising nanotechnology for replacing the CMOS in future. This work focus on the realization of logic gates using the QCADesigner and the performance measures like latency, area, and cell count were evaluated. The QDE tool is then used to gage the energy dissipation of the aforementioned circuits. Compared to conventional CMOS logic, the hybrid implementation of logic gates with spintronics achieves about 50–60% higher energy efficiency. For energy-efficient designs for high-speed applications, QCA is therefore the best substitute for CMOS logic which provides almost 90% of power reduction. Therefore, the development of logic circuits using QCA becomes significant for nano-computing and nano-communication future applications.

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