Performance Evaluation of Multiplier Architectures for FFT Processor

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Abstract: The performance investigation of various multiplier architectures has been proposed for FFT Processor design. In this article, six different multiplier designs— Booth Multiplier, Array Multiplier, Wallace Tree, Dadda Multiplier, Baugh-Wooley as well as Vedic Urdhva Tiryagbhyam (UT) multiplier, are systematically compared with respect to delay, frequency as well as power with the hardware silicon area. The Virtex6 XC6VCX75T FF484 FPGA board is used to implement numerous multiplier architectures for an FFT processor. The synthesis results show that the Urdhva Tiryagbhyam multiplier is the most suitable choice to achieve an optimized FFT Processor for a OFDM transceiver system. As compared with typical multiplier architectures, the Urdhva Tiryagbhyam vedic multiplier achieved lower hardware area as well as delay. The results of this article are useful for finding out the best and most effective multiplier topologies for implementing FFT processors.

Keywords: Vedic Muliplier; Urdhva Tiryakbhyam algorithm; Multiplier design; Hardware area; Virtex6; FPGA board; Optimized Power

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Introduction

The two most crucial computational engines are the Fast Fourier Transform (FFT) as well as the Inverse Fast Fourier Transform (IFFT) that are used in DSP systems. Some applications such as the fifth-generation wireless networks, OFDM Modulation, radar systems, MRI imaging, and audio coding require high throughput and low power FFT engine. Multipliers are the most critical components in FFT architecture and contribute significantly to hardware utilization. Conventional multiplier designs lead to increased area consumption and higher power consumption in VLSI implementation. Integration of optimized multipliers within FFT processors is essential to enhance overall system performance. There is a requirement to design an area-efficient and power-efficient multiplier architecture. Traditional adders used for summing partial products introduce additional delay and resource overhead. There is a need for faster addition techniques to handle multiple partial products efficiently.

Related work

A comparison of the Vedic multiplier employing Vedic algorithms via current multipliers with medical applications were discussed by R. Karthi Kumar and S. P. Vimal [1]. According to FFT-driven spectral analysis methods for broadband RF transceivers as well as multi-dimensional picture restoration engine

designs, complex number multiplication is an essential functional component that makes up the manipulation of digital signals [2]. This article discusses the creation and execution about an innovative QuadCross Urdhva Tiryakbhyam (QCUT) multiplier using vertical and crosswise method to enhance the efficiency for fundamental arithmetic calculations [3]. Innovative multiplier design techniques have been made possible by the Vedic Multiplier, which was inspired by old Indian mathematical methods [4]. Dhanasekar et al. [5] discussed the XOR-driven 4:2 compressor adder, which was suggested for 8-bit UT Vedic multipliers suitable image processing algorithms. Therefore, efficient computational compressor adders are needed over larger bit multiplication [6] – [8]. Six multiplier topologies are described in the Table 1 for FFT Processor.

Table 1. Comparison of various multipliers used for FFT Processor

Multiplier Type	**Inputs & Outputs**	**Methodology / Working Principle**	**Advantages**	**Area Requirement**	**Power Consumption**	**Applications**
Array Multiplier	Two unsigned binary inputs → Product	Generates all partial products simultaneously and adds them using a regular array of adders	Simple structure, regular layout, easy to design	Medium	High	Embedded systems, educational circuits, small processors
Booth Multiplier	Two signed/unsigned binary inputs → Product	Uses Booth encoding to reduce the number of partial products before addition	Reduces partial products, efficient for signed multiplication	Medium–High	Medium	DSP processors, CPUs, ALUs
Wallace Multiplier	Two binary inputs → Product	Reduces partial products using Carry Save Adders arranged in a tree	Very high speed and low propagation delay	High	High	High-performance processors, DSP, Image Processing
Dadda Multiplier	Two binary inputs → Product	Optimized reduction of partial products using fewer adders than Wallace Tree	Lower hardware than Wallace with comparable speed	Medium–High	Medium	ASICs, DSP processors, High-speed arithmetic units

Baugh-Wooley Multiplier	Two's complement signed inputs → Product	Rearranges partial products to simplify signed multiplication	Efficient signed multiplication, regular architecture	Medium	Low	Digital signal processing, Arithmetic Logic Units
Proposed Urdhva Tiryagbhyam vedic multiplier	Two signed/unsigned binary inputs → Product	Uses the Crosswise as well as vertical algorithm generate partial products simultaneously	High speed, low delay, low power, modular, regular layout	Medium	Low	DSP, FFT, AI accelerators, FPGA, ASIC, Image Processing, Cryptography

Key Contribution

The existing multiplier topologies need a significant reduction in silicon chip area. In this article, six multiplier – Array, Wallace Tree, Booth, Baugh-Wooley, Dadda Multiplier, as well as Vedic Urdhva Tiryagbhyam algorithm were discussed. The Virtex6 XC6VCX75T FF484 FPGA board was used to implement the multiplier architectures. The post-synthesis measurements like area, power and delay are extracted using the Xilinx ISE tool. The UT Vedic Multiplier of 16-bit for FFT/IFFT processors uses a novel 4-2 and 5-3 Compressor adder.

Method, Experiments and Results

The performance analysis for several multiplier architectures had been investigated for implementing the FFT/IFFT Processor. The Urdhva Tiryagbhyam (UT) sutra of Vedic mathematics computes the product of two numbers by simultaneously applying vertical (bit-aligned) and cross-wise (diagonal) partial products. Unlike classical approaches that propagate carries through adder rows sequentially, the UT sutra generates every partial product in a single step, and all column sums are computed fully in parallel. This leads to the most optimal delay and power consumption for the architecture under consideration.

The proposed design is a 16x16-bit UT multiplier configured to serve as the twiddle factor unit inside a pipelined Radix-4 FFT butterfly. The multiplier design's which were examined involve the device's LUTs, latency, slice count, power consumption as well as hardware area. As a result, the suggested multiplier design lowers the critical latency and increases design efficiency compared to the multiplier design units. Table 2 presents evaluation metrics for various multiplier topologies in addition to compressor adder-based UT Vedic Multiplier.

Table 2. Performance Metrics using Several Multiplier Architectures using Virtex6 FPGA

Multiplier	Area (LUTs)	Delay (ns)	Power (mW)	Freq (MHz)	ADP
Array Multiplier	312	18.42	42.6	54.3	5.74
Booth Multiplier	268	15.30	38.1	65.3	4.10
Wallace Tree	241	13.76	35.4	72.7	3.32
Dadda Multiplier	229	12.88	33.9	77.6	2.95
Baugh-Wooley	255	16.10	39.5	62.1	4.11
Proposed Vedic UT Multiplier	186	9.84	26.3	101.6	1.83

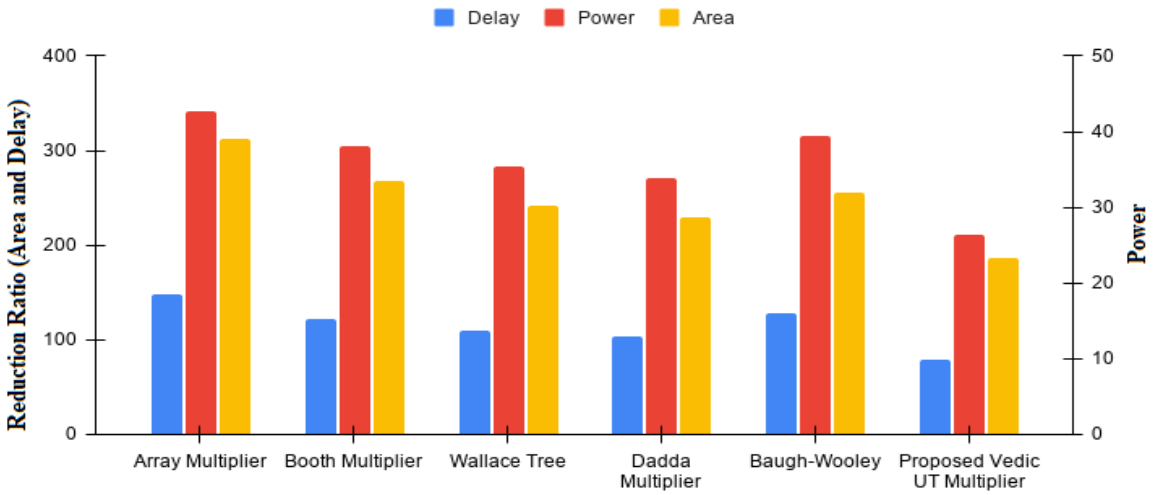

Figure 1. The existing along with proposed UT Vedic Multiplier's performance indicators including area, delay as well as power

Discussions

A number of multiplier topologies, such as the Wallace Tree, Booth, Array, Dadda, Baugh-Wooley multiplier design as well as Urdhva Tiryagbhyam multiplier, have been implemented using the Virtex6 XC6VCX75T FF484 FPGA device, that needs a smaller hardware area and power consumption. All multiplier architectures' performance metrics are shown in Figure 1. The suggested multiplier design uses a compressor adder has delay is 38% fewer, area is 27% smaller, and power is 33.4% less versus Baugh-Wooley Multiplier. The Urdhva Tiryagbhyam multiplier attains the lowest dynamic power at 26.3 mW, according to the power consumption measurements. As compared to other multiplier topologies, the suggested Vedic multiplier attains less area and power, which is best suitable to design a FFT Processor design.

Conclusions

1. In this research article, Virtex6 XC6VCX75T FF484 FPGA implementation is employed to a several multiplier topologies.

2. Based on the Xilinx ISE post-synthesis measurements report, the suggested Vedic multiplier achieves an improved silicon area as well as power consumption with reduced latency as compared to conventional multipliers.
3. In particular, the compressor adder based Vedic multiplier reduces dynamic power by 33.4% and achieves a 27% less silicon area compared to the Baugh-Wooley Multiplier. These benefits result from the Urdhva Tiryagbhyam multiplier characteristic, which reduces the hardware complexity, delay and increase the performance in FFT Processor design.
4. The compressor-based UT Vedic multiplier can be used in OFDM data communication and signal processing and it's also providing fast multiplication of data samples and twiddle factors in FFT/IFFT processors.

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