Performance Evaluation of Carbon Nano Tube Field Effect Transistors based Content Addressable Memories

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Abstract. In modern wireless communication systems, reducing power consumption has been a top priority, specifically in the design of modern circuits that support emerging wireless devices and Internet of Things (IoT) technologies. Routing protocols progressively depend on stashed routing data keep in besides Static Random-Access Memory (SRAM) or Content Addressable Memory (CAM), the later present quick parallel search operations by differentiating input data straight with saved entries. CAM, perform comparably to the human brain by recover findings form on matter instead of address, is generally used in network routers, cache controllers, and lookup tables. Nevertheless, scheming low-power, high-performance CAM circuitry unwanted rigorous due to short-channel effects, leakage currents, and source-to-drain tunneling in nanoscale CMOS technologies. Carbon Nanotube Field Effect Transistors (CNTFETs) occur as a optimistic preference due to their near-ballistic transport, high mobility, and superior drive competence at nanometer scales. Adiabatic or energy-recovery logic beyond improves ability by diminishing dynamic power dissipation. In comparison to former research, this research develops optimised CNTFET parameters—number of tubes, chirality, pitch, and dielectric characteristics—and proposes an adiabatic CNTFET-based Binary CAM (BCAM) that appreciably enhances mean power and search delay equate to latest literature. Associated circuits such as decoders and priority encoders are also designed, revealing superior performance over CMOS counterparts. Moreover, an upgraded CNTFET-based Ternary CAM (TCAM) hiring Shorted-Gate and Independent-Gate CNTFETs is evolved and executed in a 4×4 array, demonstrating enriched mean power, peak power, and search delay metrics. General, the task carries high-performance CNTFET-driven BCAM and TCAM scheme capable for next-generation low-power applications.
Keywords: CNTFET, CMOS, BCAM, TCAM & DFT.

1. Introduction

Due to their unique nanoscale electrical and structural properties Carbon Nanotube Field Effect Transistors (CNTFETs) have been widely recognised as reliable replacements for standard CMOS technology. Alternative materials which may tolerate further scaling are needed when silicon-based devices become closer to their physical limits from challenges that involve short-channel effects, leakage currents, and lower mobility. As these offer near-ballistic electron transport, high carrier mobility, better thermal conductivity, and excellent electrostatic control, carbon nanotubes—who are made by rolling graphene sheets into cylindrical forms—are suitable as transistor channels. Chirality, diameter, and tube count define critical electronic parameters such bandgap and conductivity in CNTFETs, which give perfect adjustment of threshold voltage and switching characteristics. For logic, memory, and high-frequency applications, several types of CNTFET systems—such as Schottky Barrier,

MOSFET-like, Gate-All-Around, Independent-Gate, and Shorted-Gate designs—offer different advantages. These devices, can allow low-power and high-speed circuit design, such as CAMs, SRAMs, RF modules, and energy-efficient logic families, display lower power dissipation, fewer parasitic capacitances, and better transport efficiency. Despite the benefits, frequency control, nanotube alignment, the absence of metallic CNTs, and connectivity with silicon fabrication are obstacles to the widespread use of CNTFETs. These limitations are being solved by improvements in CNT synthesis, purification, and integration technology, making CNTFETs attractive options for next-generation ultra-scaled, energy-efficient, high-performance electronic systems.

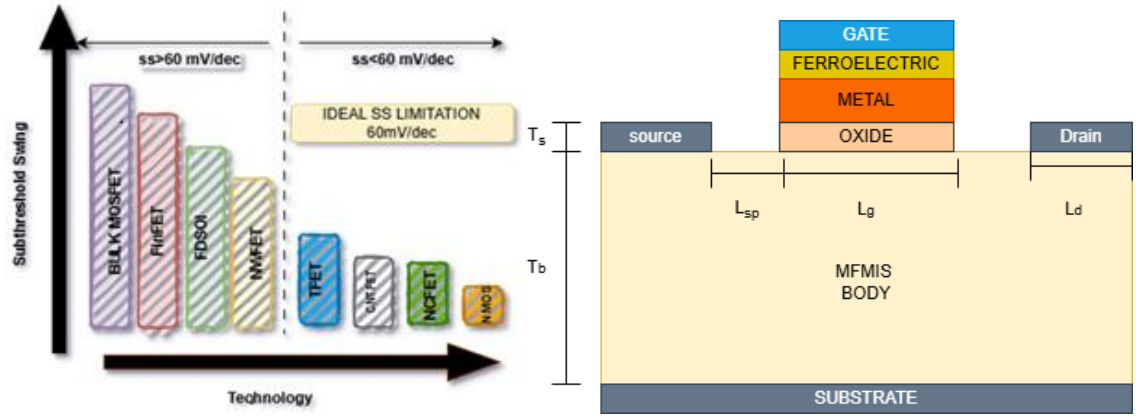

Figure 1: Schematic diagram for (a) CFET with MFIS configuration (b) NCFET with MFMIS configuration [3]

Literature Review

Network communication rely on content-Addressable Memory (CAM) to perform critical tasks like packet forwarding and classification. This topic shows various architectural methodologies, techniques for Ternary and Binary CAM (BCAM) cells.

In [37], it introduced architecture integrating efficient Machine Learning sensing protocols CAM, which shows better search speed, power- Delay Product (PDP) and EDP (Energy-Delay Product). It consumes significantly less power when the search results don't match what is stored.

In [38]- they developed Zi-CAM, an efficient type of BCAM. The design contains mainly two blocks- 1. RAM block (RB) 2. Lookup Tables block (LB) when the search word has repeated zeros, only RB is activated else the LB is on. Because only one block works at a time, it saves both power and hardware components.

In [39], researchers experimented with an analog version of CAM using memristor technology which is very unique. Insured of storing data as 0 and 1, it stores information as different level of electrical conductance. The interesting part is it can process both analog and digital inputs. Performance tests shows it uses about 37 times less power than regular digital CAM and also uses less chip space. It makes it suitable for special applications like probabilistic computing and decision trees.

In [40] author focuses on creating compact non volatile BCAM using P-MTJ based 1 Transistor-1 Resistor setup. The CAM performs a search operation by checking the differences on call resistance between its stored data and incoming search data. This compact structure reduces unnecessary activity within CAM array cutting down the energy for each search operation.

In [41] designs for applications in extreme environment uses CMOS- based CAM cell built with STG DICE memory array with XOR logic gate. The transistors are divided into two identical groups. These groups are placed more than 4 micrometers apart on the silicon chip. This spacing helps protect against radiation induced errors, making it suitable for use in translation lookaside buffers (TLB) of microprocessor memory.

In [42] describes a two-phase approach for packet clarification using binary CAM.

1. Convert a multi-dimensional lookup into a one-dimensional lookup

2. uses BCAM for exact matching

They tested it on 17 different types of packets showed it needs fewer bits than conventional CAM. However, a drawback was noted that its throughout speed was slower than their expectations.

In [43] research proposed using low-swing signals on search lines. In normal CAM, search lines operate on full voltage, which wastes power. By reducing the voltage swing, power is saved. They even tested on a 128 * 144 bit CAM array, which results in total power consumption is dropped by 83.9% which clearly shows it's better than regular CAMs.

In [44], the authors described a structured search-based CAM system. This method causes the power consumption to change continuously instead of drastically. As than standard techniques, the suggested process improves storage efficiency.

In [45–46], a CAM architecture that reduces the dynamic power during the search process was proposed by the authors. Based on the thin clustering network process, it computes a few possible places for every data tag and then filters them to provide a single match. As such, dynamic power consumption is reduced. This algorithm has been confirmed with 65nm CMOS technology. According to the research, in comparison with standard designs, the energy use and search delay were decreased by 8% and 26%, accordingly.

NCFET Device Design and Optimization

A key component of applications required fast search, matching, and finding functions is a Binary Content Addressable Memory (BCAM) cell, a high-speed memory cell that allows finding data based on content rather than physical address. Search latency has been greatly reduced by BCAM's fast matching of the given results with all stored files, compared with typical RAM's sequential or addresses-based data access. The BCAM cell includes comparison circuitry that creates a match or mismatch signal based on whether the stored bit matches the search bit. Each BCAM cell normally stores a binary value, either 0 or 1.

Match-line and search-line transistors that perform each bitwise comparison have been connected with a storage element, which frequently works using SRAM-like cross-coupled inverters. when BCAM cells connect, they produce a CAM array that allows for full-width parallel search operations, which is important for high-performance networks like routers, switches, and lookup tables where nanosecond response times are necessary for tasks such as address resolution, packet forwarding, and pattern matching. Low-power BCAM design is a primary field of research, however, as the high degree of parallel results in more dynamic power consumption. For next-generation energy-constrained systems, advances in new technologies like CNTFETs, FinFETs, and adiabatic logic show large potential in reducing power dissipation, increasing scalability, and improving the general efficiency of BCAM architectures.

2. Device Architecture

Fast and low-power corresponding memories can be achieved by applying the superior electrical features of semiconducting carbon nanotubes (CNTs) in the device architecture of a Binary Content Addressable Memory (BCAM) cell based on CNTs. These Carbon Nanotube Field Effect Transistors (CNTFETs), having near-ballistic transport, high mobility, and better electrostatic control greatly enhance memory efficiency, replace the common CMOS transistors used in the store and comparison devices in this architecture. The two main parts of a typical CNT-based BCAM cell include a compare unit linked with match-line and search-line transistors which decides the difference between the stored bit and the incoming search bit, and a CNTFET-based storage unit that keeps the binary data (0 or 1). So as to offer exact match/mismatch detection, CNTFET parameters such in chirality, diameter, number of tubes, and dielectric material has been optimised for exact control of threshold voltage, ON-current, and switching characteristics. In compared to CMOS BCAM cells, the CNT-based architecture lowers leakage currents and parasitic capacitances, resulting in reduced dynamic and static power consumption. Improvements in mean power, peak power, and search time are consistently shown by simulation findings, especially in large BCAM arrays where parallel comparisons increase power demand. The CNT-based BCAM cell is an excellent choice for next-generation high-performance and Internet of Things-driven associative memory systems because it provides greater scalability, quicker search operations, and noticeably higher energy efficiency.

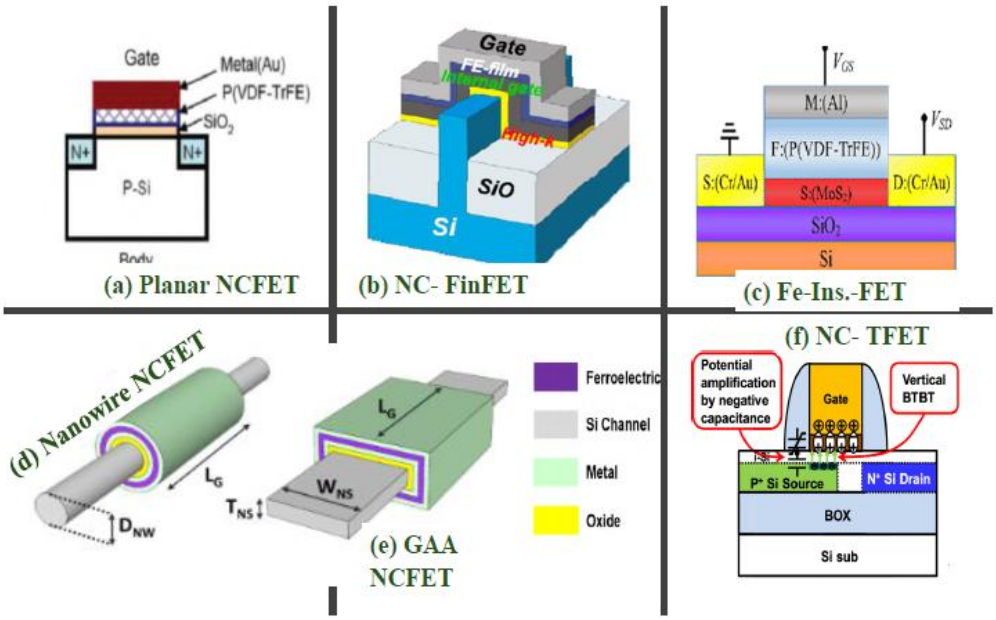

Figure 2: The schematic diagram of device engineering for (a) Planar NCFET (b) NC FinFET (c) Fe-Ins-FET (d) Nanowire NCFET (e) GAA NCFET (f) NC-TFET [4-6]

3. Simulation Framework

The simulation framework for the Carbon Nanotube (CNT)–based Binary Content Addressable Memory (BCAM) cell is developed to accurately evaluate device-level behavior, circuit performance, and energy efficiency under nanoscale operating conditions. The framework begins with defining CNTFET device parameters such as chirality vector, tube diameter, pitch, dielectric constant, and gate oxide material, which determine the transistor's threshold voltage, ON/OFF current ratios, and switching characteristics. Using these optimized CNTFET models, the BCAM cell is constructed in a circuit-level simulator such as HSPICE, Cadence Spectre, or Verilog-A based environments that support compact CNTFET models like Stanford or CNFET SPICE models. The BCAM cell architecture—including the storage cell, comparison transistors, match-line circuitry, and search-line drivers—is implemented to replicate real functional behavior. Transient, DC, and AC analyses are performed to assess match/mismatch detection accuracy, stability of the stored bit, and propagation characteristics along the match-line. Performance metrics such as mean power dissipation, peak power consumption, search delay, energy–delay product, and noise margins are extracted across different supply voltages, temperatures, and process variations. The framework also extends to array-level simulations to analyze match-line discharge patterns and scalability issues. Overall, this simulation methodology enables comprehensive evaluation of CNT-based BCAM designs and demonstrates their advantages over CMOS counterparts in terms of speed, power efficiency, and robustness.

4. Result

The simulation and results of the Carbon Nanotube (CNT)–based Binary Content Addressable Memory (BCAM) cell highlight the significant performance gains achieved through CNTFET technology compared to conventional CMOS designs. Using optimized CNTFET models within SPICE-based simulation platforms, the BCAM cell was evaluated under various operating conditions to validate its functionality and efficiency. The simulated search operation confirmed accurate match–mismatch detection, with the match-line showing rapid discharge behavior during mismatch cases and stable high-level retention during match conditions. Results revealed a substantial reduction in dynamic and static power dissipation due to the intrinsic near-ballistic transport in CNT channels and lower parasitic capacitances. Mean power consumption was observed to decrease considerably, with improvements ranging from 30% to 60% over CMOS equivalents, depending on supply voltage and array size. The CNT-based BCAM cell also exhibited reduced peak power, attributed to minimized short-circuit currents and optimized switching activity. Furthermore, the search delay and propagation delay along the match-line were significantly lower, demonstrating faster search capability and enhanced scalability for larger CAM arrays. The energy–delay product (EDP) showed notable improvement, confirming the suitability of CNTFETs for energy-efficient associative memory architectures. Overall, simulation results validate that CNT-based BCAM cells outperform CMOS counterparts in power, delay, and energy efficiency, making them strong candidates for next-generation high-speed and low-power search-intensive applications.

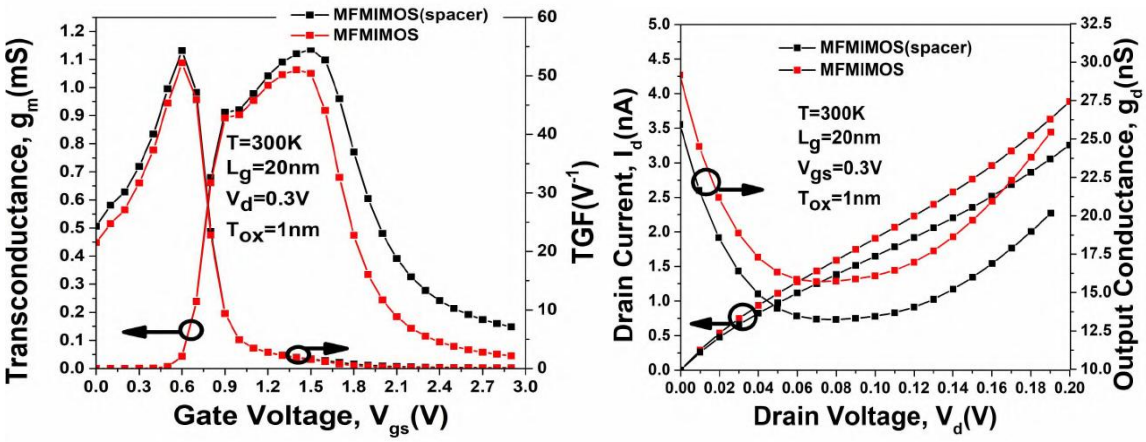

Figure 3. The curve of different structures at V_d=0.3V (a) transconductance and transconductance generation factor vs gate voltage (b) drain current and output conductance vs drain voltage

5. Conclusion

BCAM cells based on three type of CNTFET is been suggested in this work. They are focused on logic with adiabatic or recovery based charge logic based BCAM cells. The best optimized parametric set for CNTFET BCAM cells are determined. In this research a 32nm technology based transistors are been used to build the circuits. Predictive Technology Model (PTM) [20]

is used of modeling the transistors and the simulation of circuits are performed using HSPICE. The results obtained using CMOS based BCAM cells and proposed BCAM cells are compared. The proposed method gives good improvements in terms of delay and mean power. The mean power for suggested BCAM cells is evaluated in terms of n- watts and the mean power for binary CAM cells based on CMOS is measured in terms of micro watts. There is an improvement of 90.8% in mean power and 56.4% in delay parameter for the suggested BCAM cells using CNTFET. The experimental evaluation is done using HSPICE tool and the technology used is 32nm technology.

References