Performance Analysis of a Single-Stag Cascode LNA in 180-nm CMOS Technology

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Abstract: A compact RF front-end amplifier is developed for S-band communication systems using a 180-nm CMOS process. The proposed circuit adopts a single-stage cascode configuration in which source inductive degeneration is incorporated to simultaneously improve the input impedance characteristics and optimize the trade-off between amplification and noise performance. Based on schematic-level simulations, the designed LNA achieves a maximum gain of > 50 dB, whereas the simulated noise figure less than2 dB within the S-band frequency range. The design also maintains satisfactory input/output impedance matching and unconditional stability over the intended operating region. The active circuit occupies only 0.180 mm² of silicon area and dissipates approximately 52 mW of power. The combination of high gain, low noise, stable operation, and compact implementation makes the proposed architecture a promising candidate for S-band receiver front ends. Furthermore, its single-stage realization reduces circuit complexity while delivering performance that is competitive with comparatively sophisticated multi-stage LNA designs.

Keywords: Low Noise Amplifier (LNA), Figure of Merit, Noise Figure, CMOS

1. Introduction: The continuous growth of wireless communication technologies has increased the demand for compact and efficient RF front-end circuits capable of operating at microwave frequencies. Within the S-band spectrum, the 2–3 GHz frequency region is particularly significant because of its widespread utilization in satellite communication, radar, Internet-of-Things (IoT) systems, and various wireless communication platforms. In an RF receiver, signals arriving at the antenna may have extremely low power and can easily be degraded by the noise generated within the receiver itself. Consequently, the first active circuit in the receiver chain must provide sufficient amplification while contributing as little noise as possible. The Low Noise Amplifier (LNA), being one of the primary building blocks of the receiver front end, therefore plays a critical role in determining receiver sensitivity and signal-to-noise ratio (SNR) [1], [2].

Designing an LNA involves simultaneously satisfying several performance requirements that are often mutually conflicting. Adequate gain is essential for suppressing the impact of noise introduced by the circuits following the LNA, while a low noise figure (NF) is required to preserve the integrity of weak RF signals. Furthermore, effective input and output impedance matching is necessary to ensure efficient power transfer and reduce signal reflection, with 50 Ω commonly adopted as the interface impedance in RF systems. Modern wireless devices also impose strict constraints on power consumption and chip area, particularly in applications where compactness and energy efficiency are important. Although a multi-stage amplifier can be employed to achieve high overall gain, increasing the number of stages generally results in higher power consumption, larger chip area, and greater design complexity [3],

[4]. Hence, achieving substantial gain and low noise from a compact single-stage topology remains an important challenge in RF integrated-circuit design.

The evolution of CMOS technology has enabled RF, analog, and digital circuits to be integrated on a common semiconductor platform. Such integration offers advantages in terms of fabrication cost, circuit compactness, and system-level power efficiency. Despite being an established and relatively mature process, 180-nm CMOS technology continues to offer practical advantages for RF circuits operating in the gigahertz frequency range. Its characteristics make it a viable candidate for S-band LNA implementation, particularly where design simplicity, reliability, and cost-effective fabrication are important [5]. However, obtaining optimized RF performance in this technology requires careful consideration of the inherent trade-offs between gain, noise, linearity, impedance matching, power consumption, and circuit complexity [6].

This work presents the investigation of a single-stage cascode LNA intended for S-band receiver applications. The proposed architecture is based on a common-source cascode configuration incorporating inductive source degeneration. The cascode arrangement provides improved voltage gain and enhances reverse isolation between the input and output terminals. It also helps to limit the influence of parasitic feedback associated with the Miller effect. At the input side, inductive source degeneration modifies the impedance characteristics of the transistor and assists in obtaining the desired input matching condition. In addition, this technique can contribute to improved noise characteristics when the circuit parameters are appropriately selected [7]. By combining these design approaches within a single amplification stage, the proposed architecture aims to achieve the required RF performance without relying on additional cascaded gain stages.

The primary goal of the proposed design is to establish a compact single-stage LNA capable of simultaneously delivering high gain and low noise while keeping power consumption and silicon utilization at moderate levels. The circuit is designed for an S-band operating frequency and targets a voltage gain exceeding 50 dB together with a noise figure lower than 2 dB. To evaluate the robustness of the proposed architecture, detailed circuit simulations are carried out at the schematic level. In addition, process-corner analysis is conducted under FF, SS, SF, and FS conditions to examine the effect of fabrication-related process variations on the key RF parameters. The obtained results are used to evaluate the stability and practical feasibility of the proposed design. The subsequent sections present the circuit design methodology, simulation setup, performance analysis, and comparison of the proposed LNA with existing S-band LNA designs reported in the literature.

The major contributions of this research can be summarized as follows:

1. **Single-Stage Cascode Architecture:** A compact single-stage common-source cascode LNA with inductive source degeneration is proposed for S-band receiver applications, providing high gain and improved input–output isolation.

2. **Improved Impedance and Noise Performance:**
Inductive source degeneration is incorporated to facilitate input impedance matching and achieve low-noise operation, while the cascode structure helps reduce the impact of the Miller effect.

3. **High Gain with Low Power and Area:** The proposed LNA targets a voltage gain above **50 dB** and a noise figure below **2 dB**, while maintaining moderate power consumption and silicon area without using multiple amplifier stages.

4. **Robustness and Performance Evaluation:** The design is comprehensively evaluated through schematic-level simulations and FF, SS, SF, and FS process-corner analyses to assess RF performance, stability, and tolerance to process variations.

Related works : LNA has different parameters of design metric. Therefore, Figure of merit (FOM) is used to compare the overall performance of LNA. FOM includes the effect of power gain, bandwidth, linearity, NF and power dissipation and given as in equation (13)[19-20]. Different parameters comparison of proposed LNA with other work is shown in Table 2.

$$\text{FOM} = 20\log_{10}\left(\frac{S_{21av.[lin]} \times BW_{[GHz]} \times IIP3_{[mW]}}{P_{dc[mW]} \times \left(F_{av.[lin]} - 1\right)}\right) \quad (13)$$

Table 1. Performance Summary of State of Art with Proposed Work

Parameters	**[11]**	**[12]**	**[14]**	**[16]**	**[21]**	**Proposed works**
NF (dB)	2.8-3.4	3.8	2.76*	3.9-5.8	3.0#	**1.1#**
3dB bandwidth (GHz)	0.2-3.8	0.1-2.0	DC-5	1.6-9.7	0.0-1.4	2.1-3.4
S_{11} (dB)	<-9	<-12	<-12	<-14	<– 10	**<-12.4#**
P_{DC} (mW)	5.7	3	10.4	10.6	12.8	3.6
Peak Gain (dB)	19v	7.6	13.9	12.6	16.4	**17.1**
Supply (V)	1	1.2	1.8	1.8	1.2	1.0
No. of Inductors	0	0	2	6	0	**0**
Technique	Noise cancellation	Feedback	Dual feedback	Post Distortion	Shunt feedback	**Inductorless CCG-BBCS**
FOM	22v	12	-5.9	-	-9.2	**12.4**
Technology	130nm	130nm	180nm	180nm	180nm	45nm

It can be directly observed from Table 1 that proposed LNA has good result in term of NF, input reflection coefficient. Proposed LNA has sufficient bandwidth (2.1-3.4GHz) and can be used as front end circuit in wireless for UWB. The overall performance is better and can be observed by FOM as compared with the state-of-art.

2. Method, Experiments and Results

This section details the design of the single-stage Low Noise Amplifier (LNA), optimized for S-band operation in a 180nm CMOS process. The design focuses on achieving high gain and a low noise figure within a single amplification stage through careful selection of topology, device sizing, and matching networks.

2.1. Topology Selection: Cascode with Inductive Degeneration

he proposed LNA employs a **common-source cascode configuration** as its primary gain stage. This topology is particularly suitable for single-stage RF amplification because it can provide high gain and strong input–output isolation while maintaining satisfactory high-frequency operation. The cascode arrangement also suppresses the influence of the **Miller effect**, thereby minimizing unwanted feedback through parasitic capacitances and improving the stability and frequency response of the amplifier. These characteristics make the topology well suited to the requirements of lower S-band receiver front ends without the complexity associated with multiple gain stages.

A **source-degeneration inductor** is incorporated at the source of the input transistor to simultaneously address impedance matching and noise performance. The inductive element introduces a suitable resistive component into the input impedance, facilitating matching with the standard **50-Ω RF source**. In addition, appropriate selection of the degeneration inductance and transistor operating conditions helps move the amplifier toward its optimum noise-performance region. Thus, the combined use of cascode operation and inductive source degeneration enables the proposed single-stage LNA to satisfy the demanding gain, noise, and matching requirements of S-band RF front-end applications.

2.2. Circuit Implementation

The complete circuit configuration of the proposed single-stage LNA is presented in Fig. 1. The RF amplification section is realized using transistors M1 and M2 in a cascode arrangement, which forms the primary gain-producing stage. A biasing network consisting of transistor M3 and resistor R2 is incorporated to establish and maintain the required DC operating current. At the input, an external gate inductor Lg (L1 = 7.8 nH) is combined with an integrated source-degeneration inductor Ls (L2 = 600 pH) to obtain the desired impedance characteristics and RF matching. The amplifier employs a resonant load at the output to enhance the effective load impedance and consequently improve the overall gain.

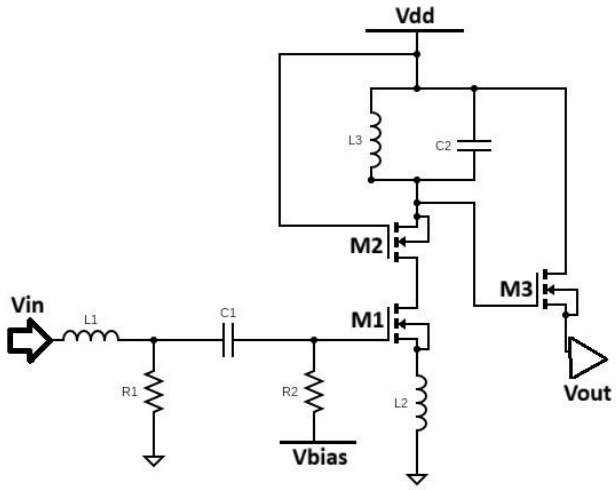


Fig. 1: Schematic of the proposed single-stage cascode LNA.

3. Simulation and Performance Analysis

he proposed LNA has been modeled and evaluated using Cadence Virtuoso based on a 45-nm CMOS process. The circuit performance is investigated over the targeted UWB frequency spectrum of 3.4–10.2 GHz. Since RF circuit performance becomes increasingly sensitive to impedance mismatch at higher frequencies, the scattering parameters are used as the primary evaluation metrics. These parameters characterize the forward transmission gain (S21), input reflection (S11), reverse transmission (S12), and output reflection (S22) of the amplifier. In addition to the S-parameter analysis, the noise figure (NF) is evaluated over the complete operating range to determine the noise contribution of the proposed amplifier.

3.1 S-Parameter Analysis

The simulated S21 and S11 characteristics of the proposed LNA over the 2.5–8 GHz frequency range are illustrated in Fig. 3.1(a). The forward transmission coefficient, S21, attains a peak value of approximately 19.8 dB at 5 GHz and maintains a relatively uniform positive response throughout the investigated frequency range. The input reflection coefficient, S11, falls below −10 dB around 5 GHz, demonstrating satisfactory input impedance matching at the selected operating frequency.

To examine the sensitivity of the proposed circuit to process variations, corner simulations are also performed for the four standard CMOS process combinations: slow-slow (SS), slow-fast (SF), fast-slow (FS), and fast-fast (FF). The corresponding S-parameter responses are presented in Fig. 3.1(b). The corner analysis provides an indication of the robustness of the proposed LNA and its ability to maintain the desired RF characteristics under variations in transistor process parameters.

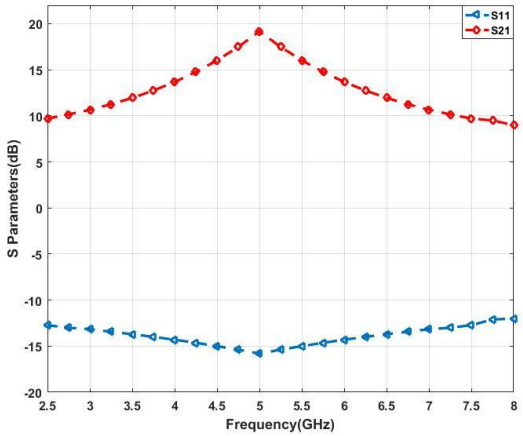


Figure 3.1 (a)

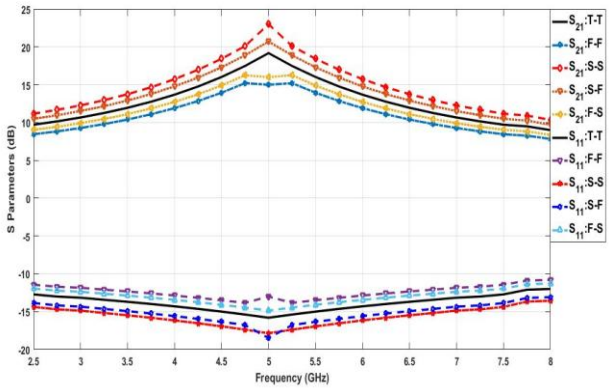


Figure 3.1 (b)

Figure-3(a)S21 and S11of Proposed LNA (b) Process corner simulation

The simulation results show that the maximum variation is no more than ten percent across the entire frequency band.

3.2 Noise Figure

The noise performance of the proposed LNA is evaluated over the frequency range of 2.5–8 GHz, as illustrated in Fig. 3.2. The simulated results indicate that the noise figure (NF) remains below 4 dB throughout the investigated frequency band, with a minimum value of approximately 1.6 dB. This low NF demonstrates the capability of the proposed amplifier to amplify weak RF signals while introducing a relatively small amount of additional noise.

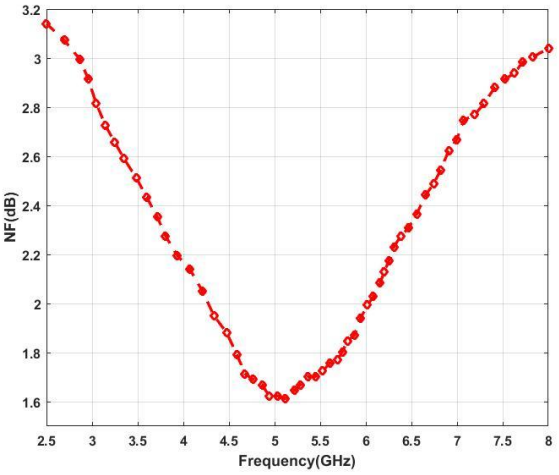


Figure 3.2 Noise Figure (NF)

Conclusions

A single-stage cascode LNA employing inductive source degeneration has been designed and investigated for 2–3 GHz lower S-band applications using 180-nm CMOS technology. The proposed architecture achieves a peak power gain of 53.23 dB, a noise figure of 1.51–1.74 dB, and input return loss ranging from

−42 dB to −5 dB, while dissipating only 45 mW from a 1.8-V supply. The obtained results demonstrate favorable reverse isolation, output matching, and unconditional stability, with the latter also verified through process-corner simulations. Overall, the proposed topology offers an attractive balance between gain, noise performance, power consumption, and circuit simplicity, making it suitable for S-band receiver front ends. Future development will focus on post-layout parasitic analysis, chip fabrication and measurement, followed by improvements in linearity, bandwidth, and integration with a complete RF receiver chain.

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