

High Gain Low Noise Figure LNA for sub-6 GHz spectrum

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Abstract: In this paper, a Low Noise Amplifier (LNA) is proposed with the objective of achieving a low noise figure, moderate gain, and low power consumption. It comprises two stages: the first is a Cascode configuration utilizing a pair of NMOS and PMOS transistors connected to share a common biasing current, thereby reducing power consumption. The equivalent transconductance of this stage is the product of the individual transconductances, resulting in increased gain. The output of the first stage feeds into a body-biased common-source stage, which enhances both gain and linearity. The frequency range from 2.5 GHz to 8 GHz was utilized for simulation purposes, conducted using Cadence software. The simulation results indicate a forward voltage gain of 19.8 dB and an input reflection coefficient (S_{11}) less than -10 dB at 5 GHz. The proposed Low Noise Amplifier (LNA) consumes 1.9 mW of power at a supply voltage of 1.5 V across the entire frequency band.

Keywords: Low Noise Amplifier (LNA), Figure of Merit, Noise Figure, CMOS

Introduction

Recent trends in wireless communication devices require multiple functions that can support all high-frequency standards within a single handset. As the number of integrated functions increases, both power consumption and chip area also rise, particularly in the transmitter-receiver integrated circuit (IC). The Low Noise Amplifier (LNA) is the first block in the receiver chain. It typically consumes a significant amount of power and is responsible for providing high gain and influencing the overall noise figure (NF) of the receiver [1-2].

Several topologies are available for designing Low Noise Amplifiers (LNAs), including: (a) distributed LNA (b) common gate LNA (c) Common source (d) Source degeneration (e) Resistive Feedback and many more [3-4].

In a distributed LNA, multiple transistors are connected in a cascade configuration, providing high gain since the final gain is the product of the individual stage gains. However, this topology consumes a large area and significant power [5].

In the common gate topology, the input impedance is the reciprocal of the transconductance and is independent of other parameters. Therefore, it is suitable for achieving a better noise figure but still consumes high power [6].

The common source (CS) topology provides high gain, which is the product of the transconductance and the drain resistance of the MOSFET. A low noise figure (NF) can be achieved in this case, as NF is inversely related to the gain of the amplifier, and the noise contribution from subsequent stages can be minimized [7].

In the feedback topology, the gain is primarily determined by the ratio of drain resistance to source resistance, enabling wideband matching. However, the receiver chain noise figure is elevated as a result of augmented white noise].

To reduce power consumption, a current-reuse topology can be employed, where a pair of N type MOS and P type MOS transistors are connected in a cascode configuration. Since both transistors share the same DC current, power efficiency is improved [9].

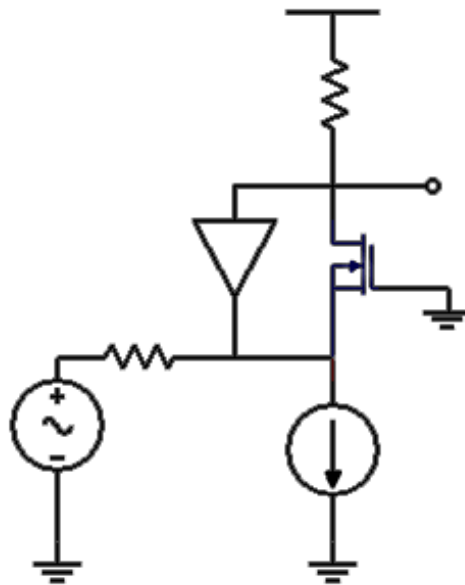


Figure 1. Shunt feedback LNA.

For improved input impedance matching, active shunt feedback can be used, as shown in Figure 1. The input impedance becomes approximately $(1 + A)$ times the impedance seen from the input terminal of the MOSFET due to the Miller effect [10]. Therefore, 50-ohm matching can be achieved by appropriately adjusting the gain A of the feedback circuit.

The proposed LNA in this paper utilizes a current-reuse technique for low power consumption, combined with shunt feedback in an active common-source (CS) amplifier [11-13].

The major contributions of this research can be summarized as follows:

1. **A wideband/UWB LNA architecture** the proposed LNA in this paper utilizes a current-reuse technique for low power consumption, combined with shunt feedback in an active common-source (CS) amplifier
2. The proposed design aims to achieve an improved **trade-off among gain, noise figure, bandwidth, impedance matching, linearity, power consumption, and silicon area.**
3. The proposed architecture is systematically evaluated using key RF performance metrics, including **S-parameters, gain, noise figure, return loss, stability, and power consumption.**

Overall, the proposed work demonstrates the potential of combining an inductive-degeneration LNA architecture with an intelligent optimization technique for the development of high-performance, low-power, and compact RF front-end circuits. The proposed approach can provide a useful design methodology for next-generation UWB and wideband wireless communication systems where high RF performance and reduced hardware complexity are simultaneously required.

Related work

Different designing parameters compared with the proposed LNA with other authors work published is shown in Table 1.

$$\text{FOM} = 20 \log_{10} \left(\frac{S_{21_{av.[lin]}} \times BW_{[GHz]} \times IIP3_{[mW]}}{P_{dc[mW]} \times (F_{av.[lin]} - 1)} \right) \quad (1)$$

Table-1

Parameters	[14]	[15]	[16]	Scope of Work
NF (dB)	1.7-2.5	3.8	2.75	4.0-1.6
bandwidth (3dB , GHz)	2.2-3.8	0.2-3.5	1.1-4.5	4.6-7.6
S ₂₁ (dB)	12	13	14.2	19.6
P _{DC} (mW)	12.6	11.2	10.4	9.2
CMOS Tech.	180	90	90	45

Key Contribution

The proposed Low Noise Amplifier (LNA) has been implemented in Cadence Virtuoso using 45 nm CMOS technology. It is designed with the objectives of achieving high gain and a low noise figure. The circuit comprises two stages: a cascode stage followed by a common-source stage. The proposed LNA achieves a forward gain of 19.8 dB at a frequency of 5 GHz, with reflection coefficients (S_{11} and S_{22}) less than -10 dB across the entire frequency band. Simulations conducted over the frequency range of 2.5 GHz to 8 GHz demonstrate an approximately flat gain response.

Method, Experiments and Results

The proposed circuit is shown in Figure 2. The circuit consists of two stages connected in cascade. In the first stage, transistors M1 and M2 are connected in a Cascode configuration. Since both transistors are connected in Cascode, they share a common biasing current.

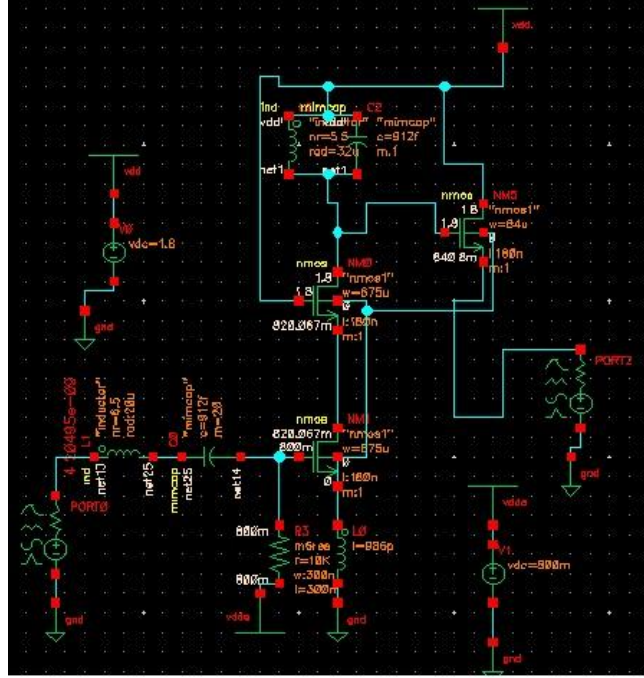


Figure-2 Proposed LNA

Henceforth, the circuit consumes low power. The voltage gain of the Cascode structure is higher compared to a conventional transistor because the overall transconductance is the product of the individual transconductances. The output of the first stage is connected to a body-biased common-source (CS) stage, thereby increasing the overall gain.

A Digital-to-Analog Converter (DAC) is used at the body terminal of the M3 transistor to control the biasing voltage. Using this voltage, a 50-ohm impedance match is achieved at the input terminal of the transistor. The voltage gain of the LNA is also controlled by the DAC. Transistors M4 and M5 form the buffer circuit. The output of the CS stage is fed to the input of transistor M4, while the output of the Cascode stage is fed to M5 through capacitor C3. The Input Impedance and gain is given by the equation2, and 3 as given below

$$Z_{in} = \frac{1}{s(C_{gs1} + C_{gs2})} \parallel \frac{(R_1 \parallel R_2)(g_1 + g + 1)}{g_{m1} + g_{m2} + g_{ds1} + g_{ds2}} \quad (2)$$

$$A_T \approx \left(\frac{Z_L(g_1 + g_{m2} + g_1 + g_{ds2})}{1 + Z_L(g_1 + g_2)(1 + sC_{gs})} \right) \cdot \left(\frac{g_{m5}(r_4 \parallel r_5)}{1 + g_{m5}(r_4 \parallel r_5)} \right) + \frac{1}{2} g_3 R_3 \frac{g_4}{g_5} \quad (3)$$

All the symbols have their usual meanings. Therefore, by using different resistors and capacitors, the gain and impedance can be controlled.

In the next section, to verify the mathematical analysis, various results such as S-parameters, Noise Figure (NF), and linearity have been simulated. To compare the performance of the proposed LNA with others, a Figure of Merit (FoM) has been used.

Result Discussions

The simulation of the proposed circuit has been carried out in Cadence Virtuoso using 45nm CMOS technology. All simulations were performed for the Ultra-Wideband (UWB) frequency range. The UWB band covers a high-frequency range from 3.4 GHz to 10.2 GHz. Since reflection increases at higher frequencies, the S-parameters, which depict performance in terms of power gain (S_{21}), input reflection coefficient (S_{11}), reverse transmission coefficient (S_{12}), and output reflection coefficient (S_{22}), have been analyzed. Additionally, the noise figure has been simulated across the entire frequency band to evaluate the noise performance.

It is observed reflections increase at high frequency. Therefore, it is important to study the simulations behavior of power gain and reflection at high frequency. Figure 3(a) represent the power gain(S_{21}) and input reflection coefficient (S_{11}) with respect to frequency range of 3GHz to 8GHz. The S_{21} is positive and S_{11} is negative throughout the frequency range. The maximum and minimum range of S_{21} and S_{11} is 17.1dB, and -16.4dB at frequency 4.1GHz.

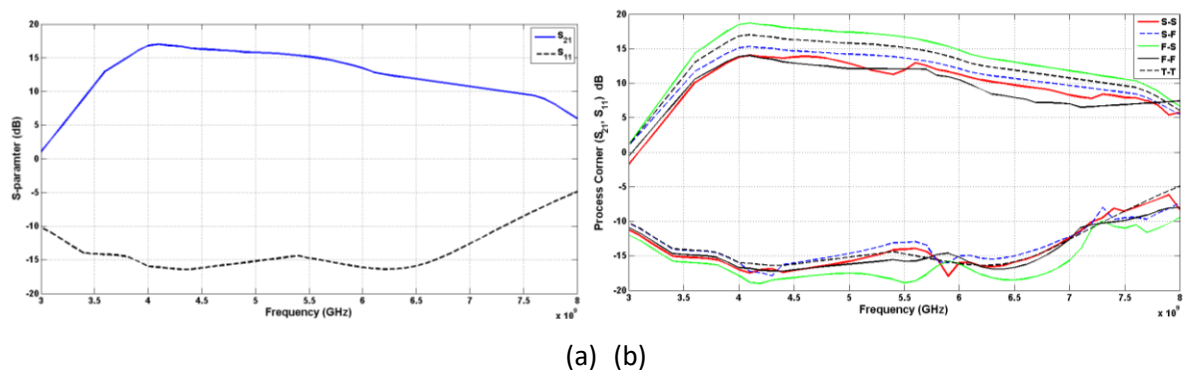


Figure 3. S-Parameters of proposed LNA (a) S_{21} and S_{11} (b) Process corner simulation (S_{21} , S_{11})

Process corner simulation represents the burst power or burst speed through all corners slow-slow, slow-fast, fast-slow and fast-fast (S-S, S-F, F-S, FF). S_{21} and S_{11} has been shown in Figure 3(b) for all corners and approx. twenty-three percent variations across the typical corner.

Noise Figure.

NF of proposed LNA as shown in Figure 4(a), for the frequency range of 3GHz-8GHz. The maximum and minimum range of NF is 4.8dB and 1.1dB simultaneously. The decrement in NF with frequency validates the mathematics of noise cancellation.

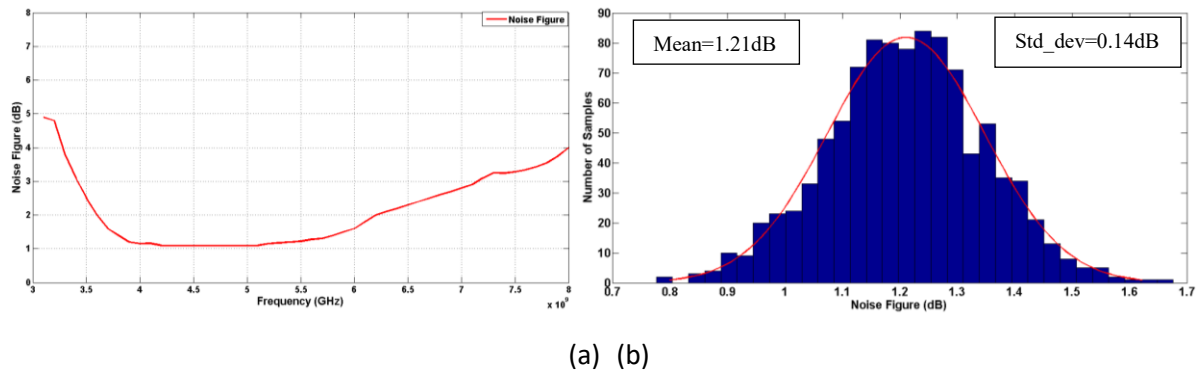


Figure4 (a) NF of proposed LNA (b) Process variation and mismatch

To check the robustness of the proposed LNA, Monte Carlo simulation has been done for NF as shown in Figure 4(b). Simulation has been done for a sample size of 1000 at frequency 4.1GHz. the mean value and standard deviation of NF is 1.21dB and 0.14dB.

Conclusions

The proposed Low Noise Amplifier (LNA) has been implemented in Cadence Virtuoso using 45 nm CMOS technology. It is designed with the objectives of achieving high gain and a low noise figure. The circuit comprises a Cascode stage followed by a common-source stage. The proposed LNA achieves a forward gain of 19.8 dB at a frequency of 5 GHz, with reflection coefficients (S_{11} and S_{22}) less than -10 dB across the entire frequency band. Simulations conducted over the frequency range of 2.5 GHz to 8 GHz demonstrate an approximately flat gain response. This performance indicates the LNA's suitability for various next-generation technology applications. Future work will focus on layout design and fabrication to realize the implementation of the LNA.

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