Design And Implementation of Spiking Neural Network Using MTJ Model

Shashidhara H R[1], Mrs. Deepthi M S[2], Prof. Sai Kiran Oruganti [3]
[1 3] Lincoln University College, Malaysia;[2] The National Institute of Engineering, Mysuru;
shashidharahr@gmail.com, ms.deepthi1391@gmail.com , saisharma@lincoln.edu.my

Abstract: Advanced non-volatile memory systems demand device models that simultaneously provide physical accuracy and computational efficiency for circuit-level integration. Spin-Transfer Torque Magnetic Tunnel Junctions (STT-MTJs) have emerged as promising building blocks for next-generation memory and in-memory computing architectures due to their non-volatility, high endurance, low standby power, and CMOS compatibility. This paper presents the design and implementation of a physics-based Verilog-A compact model for STT-MTJ devices, capable of accurately capturing magnetization dynamics, tunneling magnetoresistance behavior, and current-induced switching characteristics. The proposed model is integrated with CMOS circuitry to realize a 1T–1MTJ memory cell, enabling detailed analysis of read and write operations under transient conditions. Furthermore, the design is extended to a 2×2 MTJ-based crossbar array to investigate array-level behavior, cell selectivity, and interaction effects. Simulations are performed using Cadence Spectre with 180-nm CMOS technology, demonstrating reliable magnetization switching, stable non-volatile data retention, and consistent electrical characteristics across different operating conditions. The results validate the effectiveness of the developed model as a compact and scalable framework for STT-MRAM design and emerging spintronic in-memory computing applications.

Keywords: Spike Neural Network; MTJ; MRAM; Spin-Transfer Torque Magnetic Tunnel Junctions; MTJ-based crossbar array;

Introduction

The rapid advancement of semiconductor technology has increased the demand for memory systems that offer high speed, low power consumption, and long-term data retention. Conventional charge-based memories such as SRAM, DRAM, and Flash face several limitations including leakage power, volatility, limited endurance, and scaling challenges [1][2]. These issues have motivated the exploration of alternative memory technologies that can overcome the shortcomings of traditional approaches.

Spintronic devices, which utilize the spin of electrons in addition to their charge, have emerged as promising candidates for next-generation memory systems. Among these devices, the Magnetic Tunnel Junction (MTJ) plays a central role and serves as the fundamental storage element in Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM) [3][4]. MTJs offer advantages such as non-volatility, high endurance, fast switching, and compatibility with CMOS technology, making them suitable for future memory and logic applications.

A Magnetic Tunnel Junction consists of two ferromagnetic layers separated by an ultra-thin insulating tunnel barrier, typically magnesium oxide [5]. One of the ferromagnetic layers has a fixed magnetization direction and is referred to as the pinned layer, while the other layer is known as the free layer, whose magnetization can be switched. The resistance of an MTJ depends on the relative orientation of the magnetizations of the pinned and free layers [6]. When both layers are aligned in the same direction (parallel state), the MTJ exhibits low resistance. When they are aligned in opposite directions (anti-parallel state), the resistance increases. This resistance difference enables binary data storage, where each state corresponds to a logic '0' or '1'.

Related Work

Experimental characterization of MTJ devices is costly and time-consuming. Therefore, compact modelling approaches are widely used to study MTJ behaviour before fabrication [7]. Verilog-A is commonly employed for MTJ modelling because it allows the description of device physics using behavioural equations and enables seamless integration with CMOS circuits. In this work, a Verilog-A based MTJ model is used to analyze the dynamic switching behaviour of the MTJ at the circuit level. The model is derived from the Landau–Lifshitz–Gilbert (LLG) equation with additional spin-transfer torque (STT) terms[8][9]. The implementation is divided into two main parts: the MTJ model block and the initial condition block. Together, these blocks enable realistic simulation of magnetization dynamics, resistance variation, and switching stability. The initial condition block defines the starting orientation of the free-layer magnetization before transient simulation begins. This is essential because, in real physical devices, magnetization always starts from a well-defined state. Parameters such as the Boltzmann constant and temperature are used to account for thermal effects present at room temperature [10]. These parameters influence the initial angular deviation of the magnetization vector and represent thermal agitation in practical MTJ devices. The saturation magnetization determines the maximum magnetic moment of the free layer, while the anisotropy field defines the preferred or easy axis of magnetization. The geometrical parameters—length, width, and thickness—define the volume of the free layer, which directly affects thermal stability, switching dynamics, and noise sensitivity. Using these parameters, a small deviation from the easy axis is introduced during initialization. In this work, the magnetization components are initialized such that Mx and My have small non-zero values, while Mz is close to unity [7][9]. This ensures normalization of the magnetization vector and allows natural processional motion to occur during switching. The MTJ model block includes parameters that describe magnetic dynamics, electrical behaviour, and thermal effects. The Gilbert damping factor (α) controls how quickly the magnetization loses energy and reaches a stable state [8]. Lower values of damping lead to longer oscillations, while higher values suppress oscillations more rapidly. The gyromagnetic ratio determines the speed of magnetization precession around the effective magnetic field. The parallel resistance and tunneling magnetoresistance ratio (TMR) define the electrical characteristics of the MTJ, enabling clear distinction between parallel and anti-parallel resistance states [6]. The spin-transfer torque coefficients describe how efficiently the spin-polarized current transfers angular momentum to the free layer magnetization. Proper selection of these parameters ensures controlled and directional switching [3], [4]. An external bias magnetic field is introduced to assist switching. Simulation results indicate that moderate bias field values result in stable switching, while higher bias values cause excessive processional motion and instability. Thermal noise is modeled using a Gaussian random field derived from temperature, damping factor, saturation magnetization, and device volume [10], [11]. This allows the model to capture realistic thermal fluctuations. The magnetization of the MTJ free layer is represented using three normalized directional components: Mx, My, and Mz, which together form a unit magnetization vector satisfying: $Mx^2 + My^2 + Mz^2 = 1$ During the initial phase of switching, Mx and My exhibit oscillatory behavior due to the processional motion of magnetization around the effective magnetic field [8], [9]. These oscillations represent the transient response of the system and store excess magnetic energy during switching. As time progresses, the damping factor causes these oscillations to gradually decay, and both Mx and My approach zero, indicating that the magnetization has aligned along the easy axis and reached a stable equilibrium state. The Mz component represents the primary data storage direction of the MTJ [3], [5]. A value of Mz ≈ +1 corresponds to one stable magnetic state, while Mz ≈ −1 corresponds to the opposite state. Successful MTJ switching is confirmed when Mz transitions from +1 to −1 and remains constant thereafter. While oscillations during the transition are expected, sustained oscillations indicate instability. Simulation results show that for higher bias magnetic field values (for example, hbias = 50), Mz stabilizes after switching. However, for lower bias values (hbias = 10), Mz continues to oscillate, preventing stable data storage. This highlights the importance of proper parameter tuning for reliable MTJ operation.

Key Contribution

The following are the key contribution of the proposed work,

- The study and development of STT MTJ model.
- The characteristic study of the STT MTJ model.
- The development of 2x2 SNN Cross bar array using STT MTJ model.

Method, Experiments and Results

Modelling of MTJ: An MTJ consists of two ferromagnetic layers separated by an ultra-thin insulating tunnel barrier, typically magnesium oxide (MgO). One of the ferromagnetic layers has fixed magnetization and is referred to as the reference or pinned layer, while the other layer has a free magnetization that can be electrically switched between two stable states. The two possible magnetization configurations are: Parallel (P) state, which corresponds to a low-resistance state, Antiparallel (AP) state, which corresponds to a high-resistance state. This resistance difference enables binary data storage and is quantified using the tunneling magnetoresistance (TMR) ratio. An MTJ device typically comprises the following layers: Pinned (reference) layer: Magnetization is fixed using exchange bias or synthetic antiferromagnetic structures. Tunnel barrier: Ultra-thin MgO layer with thickness of approximately 1 nm. Free layer: Magnetization can be switched by external stimuli. The MTJ structure and its resistance states are illustrated in Fig. 1. The MTJ model module represents the complete STT-MTJ device, including three electrical terminals (positive, negative, and neutral) and internal nodes corresponding to the magnetization components mx, my, and mz. The electrical behavior is modeled by calculating the voltage-dependent resistance using the parallel resistance and the tunneling magnetoresistance ratio. The resistance dynamically changes with the magnetization state, enabling correct modeling of parallel and antiparallel configurations. Figure 2 shows the complete simulation schematic of the STT-MTJ implemented using the Verilog-A compact model. The MTJ is represented as a three-terminal device with internal magnetization nodes. Voltage sources are applied to provide read and write stimuli, and an initialization block defines the initial magnetization state. Series resistors and capacitors are included to ensure numerical stability and to realistically model the electrical interface with CMOS circuitry.

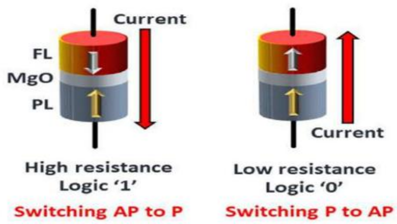

Figure 1: MTJ Device

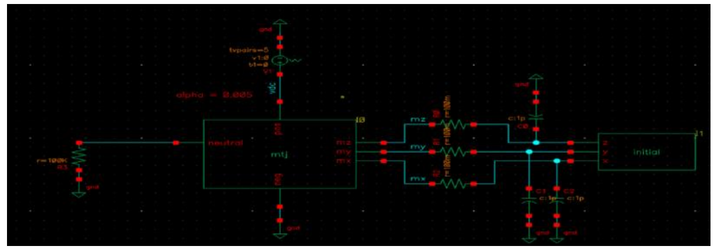

Figure 2: MTJ Schematic

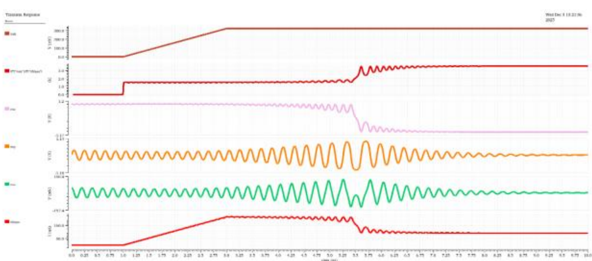

Figure 3 Transient Simulation of MTJ model

Figure 4 Resistive analysis of MTJ model

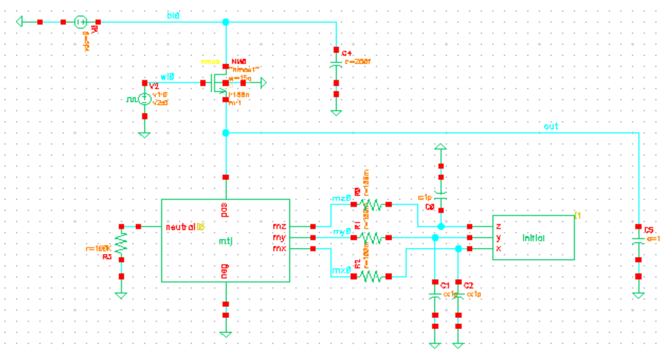

Figure 5 1T-1MTJ Schematic

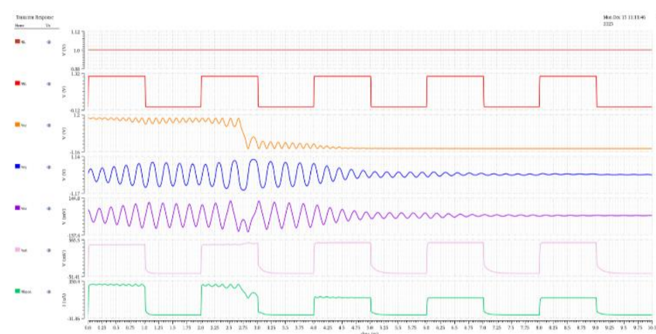

Figure 6 Transient Simulation

The 1T-1MTJ cell consists of one NMOS access transistor connected in series with one Magnetic Tunnel Junction (MTJ) [5]. This structure is preferred because the access transistor improves cell selectivity, limits leakage, and prevents sneak-path currents (Sneak-path currents are unwanted current flows through unselected memory cells in an array, and the access transistor prevents these by isolating the MTJ when the word line is inactive) in memory arrays [10]. The word line (WL) controls the gate of the access transistor and determines whether the cell is selected [5]. When the word line is high, the transistor turns ON and enables current flow through the MTJ, whereas a low word line keeps the cell electrically isolated from the bit line. The bit line (BL) is used to apply the required voltage or current for memory operation [7], while the source line (SL) provides the return path for current during operation. By controlling the voltage applied to the bit line, the amount and direction of current flowing through the MTJ can be regulated, which is essential for both sensing and switching operations. The MTJ stores information using resistance states based on the relative magnetization of its free and pinned layers [7]. A parallel alignment produces a low-resistance state, whereas an antiparallel alignment produces a high-resistance state [10]. These resistance states remain stable even after power is removed, enabling non-volatile data storage with low standby power consumption [7]. Due to the presence of the access transistor, unwanted current flow through unselected cells is minimized, which improves reliability and ensures correct operation in larger memory arrays [10].

MTJ-BASED 2×2 CROSSBAR ARRAY DESIGN: The proposed 2×2 MTJ-based crossbar array consists of four identical 1T-1MTJ memory cells arranged in two rows and two columns, where each cell is located at the intersection of a word line (WL) and a bit line (BL) [1], [2]. The gate of the NMOS access transistor is driven by the word line, while the MTJ is connected between the bit line and the source line, enabling controlled current flow through the selected cell [3]. Crossbar architectures are widely adopted in STT-MRAM due to their high memory density and compact layout, achieved by sharing horizontal and vertical interconnects among multiple cells [4]. The regular and repetitive structure of the crossbar allows straightforward scalability from small arrays to larger dimensions without altering the basic cell topology [1]. Incorporating an access transistor with each MTJ improves cell selectivity and effectively suppresses sneak-path currents, which are a major concern in passive crossbar arrays [2], [5]. This structure provides a reliable platform for studying array-level behavior, including selection, isolation, and current distribution. The 2×2 crossbar connects four 1T–1MTJ cells with shared word and bit lines, while each cell remains individually controllable via access transistors. Activating a word line selects the corresponding cell, allowing current to flow only through it. Unselected cells stay isolated, ensuring proper connectivity and reliable cell selection. In the implemented 2×2 crossbar array, bit lines (BL0, BL1) are arranged row-wise and word lines (WL0, WL1) column-wise, controlling the gate terminals of NMOS access transistors. Word lines are driven by a pulse voltage (Vpulse = 1.2 V) to select columns, while bit lines are biased with a DC supply (VDC = 1 V) to enable current flow through the MTJs. During simulation, only one word line is activated at a time, turning ON the corresponding transistors and allowing current through the selected MTJ cells, while unselected columns remain isolated. The array outputs are monitored at MZ0 - MZ3, representing the z-component of magnetization of each MTJ. These outputs confirm correct cell selection and isolation, validating the functionality of the crossbar design. Case1:BL0=0,BL1=0. Both bit lines are at logic ‘0’, so no voltage is applied across the MTJs. Even if a word line is turned ON, very little current flows, and MZ0–MZ3 remain the same. This shows that no switching occurs in the array.

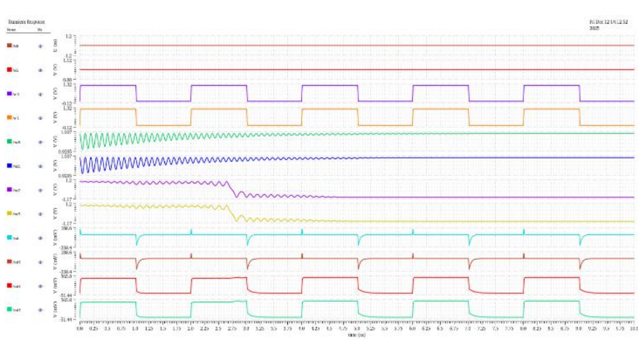

Fig.7.Simulation results for BL0=0 and BL1= 0condition

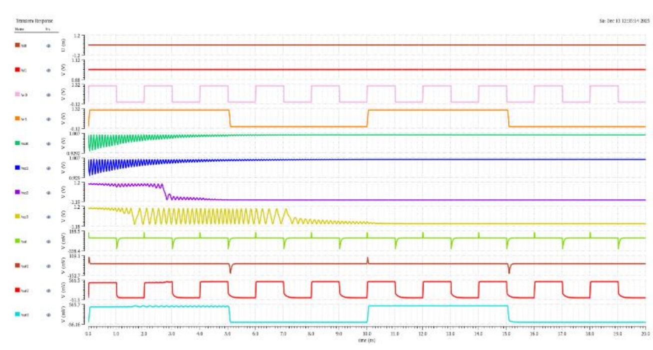

Fig.8.Simulation results for BL0=0 and BL1=1condition

Case2:BL0=0,BL1=1: Only BL1 is high, so when the word line is activated, the MTJ connected to BL1 switches. Other MZ outputs remain unchanged, confirming correct bit line selection.

Case3:BL0=1,BL1=0:BL0 is high while BL1 is low. When the corresponding word line is activated, current flows only through the MTJ connected to BL0. The associated MZ output reflects the change in magnetization, while the unselected MTJs remain unaffected. This confirms correct selective access in the array. Case4:BL0=1,BL1=1:Both bit lines are high. When the word line is activated, both MTJs in the selected column receive bias and switch. The corresponding MZ outputs change from +1 to -1, indicating successful simultaneous switching of the selected cells.

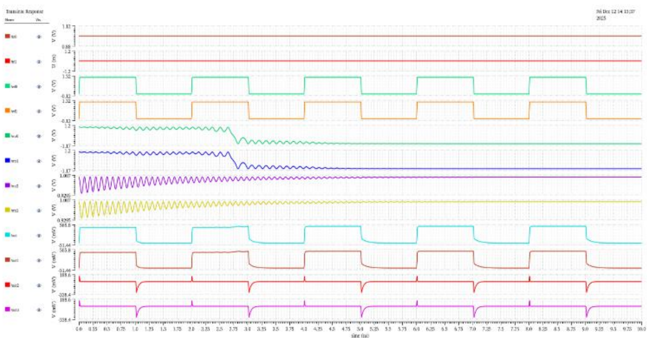

Fig.9. Simulation results for BL0 = 1 and BL1 = 0

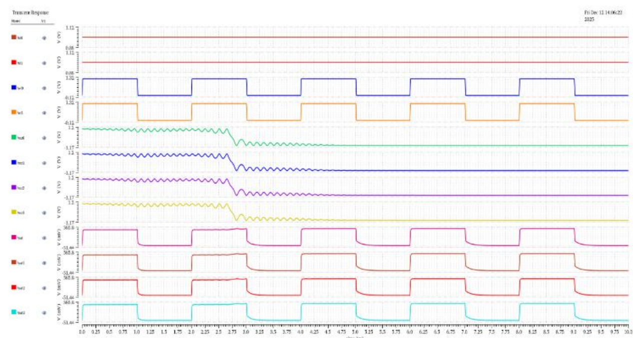

Fig.10. Simulation results for BL0 = 1 and BL1 =1

Conclusions

This paper presented a compact Verilog-A based modeling framework for Spin-Transfer Torque Magnetic Tunnel Junctions (STT-MTJs) and demonstrated its integration with CMOS circuitry. The proposed model accurately captures magnetization dynamics, tunneling magnetoresistance behavior, and current-induced switching. A 1T–1MTJ memory cell and a 2×2 MTJ-based crossbar array were designed and simulated using 180 nm CMOS technology in Cadence Spectre. Simulation results confirmed reliable magnetization switching, stable non-volatile data retention, and correct cell selectivity at both device and array levels. The work validates the suitability of the proposed approach for circuit-level analysis of STT-MRAM and magnetoresistive computing systems.

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