Power Modelling of FPGA Implementations at System Level: A Review

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Abstract: Given the recent popularity of FPGAs in performance-critical applications, power has become a top-level design constraint. While flexibility, parallelism and shorter time-to-market of FPGAs are attractive characteristics, they consume much higher power than comparable ASIC solutions making accurate early-stage power evaluation necessary. In this paper, reviews on power model and estimation in FPGA implementation are addressed with special focus on system level power estimation. Different power estimation techniques known from literature like probabilistic, statistical, simulation-based, and analytical methods were explored at various levels of abstraction. The work focuses on RTL-level and IP-based modeling techniques, regression and machine learning-based iterations, and their capacity to model dynamic power consumption. The review highlights the drawbacks of current system-level power estimation techniques, specifically their failure to accurately account for interconnection effects and power reduction in multi-IP systems. The findings indicate that while individual IP power models have achieved high accuracy, system-level estimation remains an open research challenge.

Keywords: Power Estimation; Power Modeling; FPGAs; IP Modeling; Regression

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Introduction

High-performance hardware peripherals and embedded processor cores on a single chip with conventional optimization capability have not only established Field Programmable Gate Arrays (FPGAs) as powerful System-on-Chip (SoC) but have also opened the gate for FPGAs to be utilized in many complex digital applications [1]. FPGAs are the first choice of Advanced Driver Assistance Systems (ADAS) owing to their high-level processing and fine-grain parallelism [2]. A few recent developments in the FPGA industry include Agilex M-series FPGAs launched by Intel Corporation in March 2022 dedicated to data centers, radar, and aerospace applications, Titanium TI180 FPGA launched by Efinix Inc. August 2022 dedicated to automotive and Virtual Reality (VR) applications. It has been reported that the revenue forecast of FPGAs in 2027 is approx. USD 18.8 billion [3]. Nowadays, FPGAs are the first choice of designers in comparison to ASICs counterparts due to their reconfigurability, less design turnaround time, and high operating speed. However, they consume more power, approximately 14 times more in comparison to ASICs. Power is an important parameter that needs to be taken into consideration while designing a circuit and/or a system. The available commercial tools could estimate the power after undergoing the entire design cycle which is indeed a time taking process. Hence, accurate power estimation of circuits and/or systems at an early design cycle has become a necessary requirement.

Background and Motivation

Several power estimation strategies have been documented in the literature. Probabilistic techniques estimate power based on input signal probabilities to compute switching activity [9-10], but they do not account for glitching and propagation delays, resulting in limited accuracy. Statistical techniques assess power by simulating designs with randomly generated input patterns [7-8], but they have a long runtime because to the enormous input vectors. Monte Carlo simulation approaches help to overcome this issue by reducing simulation complexity [9]. Analytical power modeling and macro-modeling are commonly used at the RTL level. Macro-modeling methods estimate power using lookup tables or equations derived from input statistical parameters [10]. Analytical power modeling techniques often leverage machine learning to build models based on selected design parameters. Several such models have been proposed in the literature. C. H. Gebotys et al. introduced a linear regression-based power model using DSP script-derived variables, achieving an estimation error below 4% [11]. S. Gupta et al. proposed a table-based power model capable of estimating circuit power for arbitrary input/output signals, constructed automatically through a gate-level characterization process [12]. N. Julien et al. developed an architectural-level power model for processors based on functional analysis and validated it using the Texas Instruments TMS320C6201 processor [13]. A. Amira et al. presented an FPGA-based implementation of the Fast Hadamard Transform using a hybrid of Handel-C2 and parameterized VHDL cores, exploiting parallelism and pipelining to achieve high throughput [14]. R. Jevtic et al. proposed a regression-based power estimation model for embedded multipliers using switching activity derived from dataflow graph simulations, achieving an average error of 8.19% on Xilinx Virtex-II Pro devices [15]. L. Deng et al. developed area and power estimation models using curve fitting and regression for the Virtex-2Pro FPGA family, reporting varying estimation errors depending on the design type [16]. A. N. Tripathi et al. proposed an ANN based dynamic power estimation model for Zynq devices, where by considering a DSP block usage as an added input feature the accuracy of the model was improved [17]. G. Verma et al. subsequently revealed deficiencies in Deng et al. 's approach as well as proposed improved regression-based methods [18]. While most existing models focus on estimating the power of individual IP cores, limited research addresses system-level power estimation involving interconnected IP cores. X. Liu et al. introduced a hybrid power estimation approach that integrates high-level simulation with macro-modeling, implemented as the Hybrid Power Estimation (HyPE) tool, achieving an average error of 7.3% for large-scale designs [19]. D. Elleouet et al. proposed a system-level power estimation identity in which total power is computed as the sum of the dynamic power of individual IP cores and FPGA configuration power. However, the omission of interconnection effects resulted in estimation errors exceeding 10% for systems comprising multiple IP cores [20]. J. Lorandel et al. extended this methodology but similarly neglected interconnection power, reporting a maximum error of approximately 5% [21]. Y. A. Durrani et al. incorporated interconnection effects but still reported errors ranging from 9% to 15%, and did not address frequency scaling or cross-device compatibility [22]. Y. Nasser et al. introduced a low-level power estimation method by decomposing digital systems into primitive operators with an error less than 8% [23]. Fewer works have considered power estimation techniques, existing studies tend to narrow down the focus on power minimisation. B. Pandey et al. demonstrated power reduction in ALUs using latch-free clock gating but did not address system-level power estimation [24]. G. Verma et al. developed accurate models for circuits employing clock-enable power reduction techniques, though system-level estimation was not considered [25]. S. Huda et al.

proposed clock gating and placement algorithms to reduce clock network power by up to 50% [26], while J. Shinde et al. analysed various RTL-level clock gating strategies and identified latch-based clock gating as the most effective [27].

Power Estimation Approaches for FPGAs

Power estimation techniques reported in the literature can be broadly classified into probabilistic, simulation-based, and statistical approaches. Probabilistic methods allow rapid power estimation but sacrifice accuracy [4]. In contrast, simulation-based techniques offer highly accurate power estimates, although they require significant time to produce power reports for a given design. Statistical approaches provide a balance between speed and accuracy, generating power estimates with moderate precision and computation time [4]. Moreover, statistical power estimation methods are suitable for evaluating the power consumption of individual IP blocks as well as complete systems formed by integrating multiple IP cores.

Power Estimation at System Level for FPGAs

The IP-based systems are implemented by connecting the needed IP cores. Power estimation for the IP-based system is performed using the Vivado design flow. Additionally, the power consumption of individual IP cores is estimated using the same flow. Post-synthesis data is utilized to develop power estimation models for individual IP cores. This post-synthesis data is provided as input to MATLAB, where regression-based power models are generated for each IP core. The developed power models are validated by comparing their results with power values obtained from a commercial tool. Once the power model for each individual IP core is established, the estimated power values are used to calculate the overall system power using the approach proposed by D. Elleouet et al [20]. According to him, the power consumption of a system composed of N IP cores can be estimated by summing the dynamic power of each IP core along with the power of the FPGA configuration plane, as expressed in Equation (1).

$$System\ power = \sum Dynamic\ power\ of\ each\ IP + Power\ of\ FPGA\ configuration\ plan \quad (1)$$

Conclusions

This paper has presented a detailed review of power modelling and estimation techniques for FPGA implementations, with a focused discussion on system-level power estimation using IP-based design methodologies. The paper also compared various power estimation strategies at multiple levels of abstraction such as probabilistic statistical, simulation based, regression, and machine learning based methods and discussed their strength and weakness. When considering the related work, most of the previous research has been focusing on predicting the power consumption of each IP core and reported promising accuracy. But, system-level power estimation of FPGA-based design consisting of interconnected IP cores is comparably unexplored. Accordingly, there is a strong need for scalable system-level power estimation methodologies that takes the interconnect power and power-aware

synthesis into account. Further work in this direction can help to enhance the accuracy of early power estimation and support the design of FPGA-based, low-power systems.

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