System Level FPGA Power Estimation: Evaluation and Analysis of Existing Models

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Abstract:

Field Programmable Gate Arrays (FPGAs) are increasingly used as the platforms of choice for both modern embedded and high-performance computing. Nevertheless, the estimation of the local power consumption at the system level remains a difficult problem, especially in the case of multiple IP cores. This paper reviews the existing FPGA power estimation methods and their application to different architectures. In particular, the evaluation of system-level power estimation models for cascaded and non-cascaded architectures is highlighted. Experimental results show that conventional IP-summation models can achieve acceptable accuracy for non-cascaded systems but incur large estimation errors for cascaded systems as a result of the propagation of switching activity between IP cores. Therefore, this paper presents a modified estimation identity, which takes into account the effect of intermediate IP cores in cascaded architectures. This paper shows that architectural dependencies can have a large impact on the accuracy of power estimation. In addition, this work highlights gaps of the current approaches in research, especially the lack of integrated frameworks that combine IP-level modeling, system-level scalability, and runtime power optimization techniques. The results provide guidance towards accurate and scalable FPGA power estimation approaches for complex heterogeneous systems.

Keywords: FPGA, Power Estimation, System-Level Modeling, Cascaded Architecture, IP Cores, Low Power Design

Introduction

Probabilistic, analytical/simulation-based and statistical power estimation techniques for FPGA-based and IP-integrated systems are compared with respect to their advantages and disadvantages in figure 1. Probabilistic power estimation techniques estimate the dynamic power by applying switching activity factors derived from the signal probabilities and thus they are fast and suitable for early design stages. However, the use of simplifying assumptions (e.g., signal independence) limits their accuracy in multi-IP systems [1-3]. Analytical and simulation methods give more accurate predictions by computing switching activity and power consumption using RTL, gate-level, or post-layout information, but are expensive in terms of computation and are usually limited to modeling individual IP cores or aggregating at the system level without modeling inter-IP interactions or are less detailed at the IP level [4]. IP-level models can accurately predict power consumption with and without local power reduction techniques such as clock gating. When multiple IP blocks are integrated to form a complete system, power is typically summed from individual IP contributions, without consideration of shared resources such as clocks, interconnects, and memory subsystems [5-8]. In this paper, we propose a hybrid power estimation framework that

combines analytical power equations with correction models, models IP- and system-level power with correlated IPs, and enables integration of power management techniques. The major contributions of our research are: (i) We present a hybrid power estimation methodology that combines analytical power equations with correction models for power estimation, (ii) We model correlated IPs, such that power estimation can be performed with IP and system-level granularity, and (iii) We present a framework that can be used to integrate power management techniques. The evaluation of our proposed framework against existing power estimation methods for two different benchmarks shows that our hybrid framework produces power estimates that are more accurate and have better scaling properties with IC- and system-level granularity, as well as providing better workload dependency [9-10].

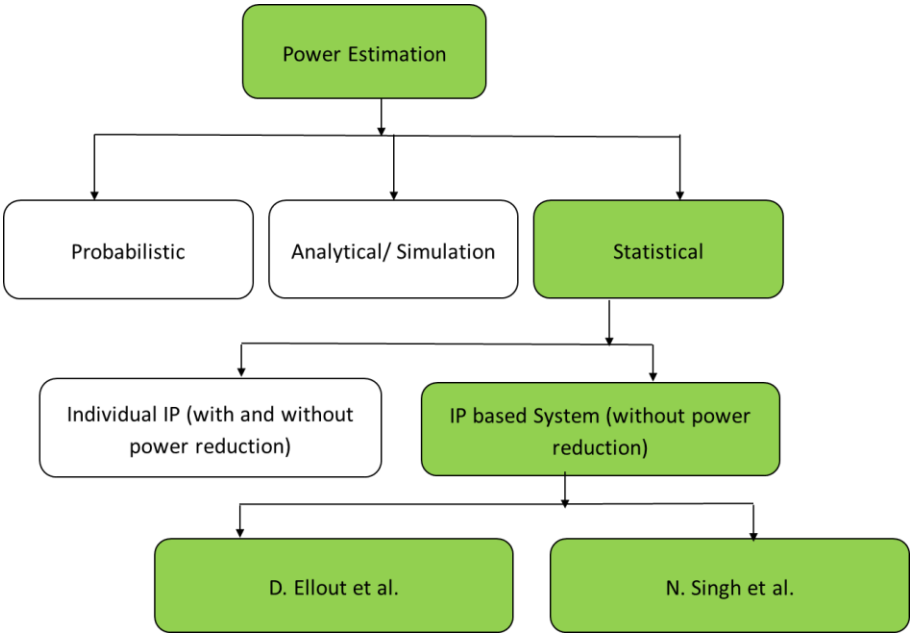

Figure 1. Power Estimation Techniques for FPGAs at Individual IP and System Level.

Cascaded and Non-Cascaded Systems

Non-cascaded and cascaded architecture systems play an essential role in Digital Signal Processing (DSP) block and logic circuit design on Field-Programmable Gate Arrays (FPGAs). Power, resource usage and performance are affected based on data flow between Intellectual Property blocks (IP cores). In a cascaded system, IP cores are connected in series or a "daisy-chain" fashion. Examples: FIR Filters, Multiply-Accumulate (MAC) Units, Arithmetic Logic Units (ALUs), Barrel Shifters, Carry Save Adders, and Serial-In Serial-Out (SISO) registers [10]**.** In a non-cascaded (or parallel) system, IP cores do not strictly depend on the previous block's output for input. Instead, outputs from each level can be obtained by applying external inputs to different intermediary blocks [10]. Examples: Carry Ripple Adders, Carry Skip Adders, Serial-In Parallel-Out (SIPO) registers, Parallel-In Parallel-Out (PIPO) registers, and Parallel-In Serial-Out (PISO) registers.

Evaluation of Existing Power Estimation Models

According to D. Elleouet et al. [9], the power consumption of a system composed of N IP cores can be estimated by summing the dynamic power of each IP core along with the power of the FPGA configuration plane, as expressed in Equation (1).

$$System\ power = \sum Dynamic\ power\ of\ each\ IP + Power\ of\ FPGA\ configuration\ plan \quad (1)$$

The proposed identity has been applied to estimate the power of different systems. It has been observed from the obtained result that the identity is providing results aligned with the Vivado results. However, for other systems the results obtained are deviating and are not aligned with the Vivado. To discover the reason behind this conflicts, architectural details of the various system were analysed. It has been found from this study that the identity is producing accurate result for systems possessing parallel (non-cascaded) architectures However, for systems with cascaded design, the identity is yielding erroneous results. In this work, a system is deemed non-cascaded if it produces output concurrently at every level. On the other hand, a cascade system is one in which the input is applied at one IP core, the output serves as the input to the middle IP cores, and the final output is taken at a different end.

According to N. Singh et al. [10], suppose a cascade system consists of N IP cores with input applied to the input stage IP core i.e., IP-1 and output is taken at output stage IP core i.e., IP-N. The output of the input stage IP is the input to the middle stages. Therefore, in this work assuming the system as a black box, the activity at the input of the input stage IP/IPs has been assumed to be directly propagated to the output of the output stage. Because of this, it has been assumed that the output power of the input stage IP cores and middle stage IP cores contributes zero to the overall power of a cascade system. Based on this idea, Equation (2) provides the identity suggested in this study that can rapidly and precisely estimate the power of systems made up of N-IP cores.

$$System\ power = \sum Dynamic\ power\ of\ each\ IP - \sum \boldsymbol{Interconnection\ power} + Power_{(FPGA\ Configuration\ Plan)} \quad (2)$$

In a cascade system, $\sum \boldsymbol{Interconnection\ power}$ is defined as the output power of the input stage IP and middle stage IP.

Analysis and Research Gap

Although significant progress has been made in IP-level and system-level FPGA power estimation [11-15], existing methodologies either focus on individual IP optimization or system-level aggregation without incorporating dynamic power reduction strategies. Furthermore, inter-IP correlation effects and workload-dependent behavior remain inadequately modeled. Therefore, there is a clear need for a hybrid IP-based system-level power estimation framework that integrates statistical modeling with runtime power reduction mechanisms to enable accurate, scalable, and design-space-aware power prediction techniques as shown in figure 2.

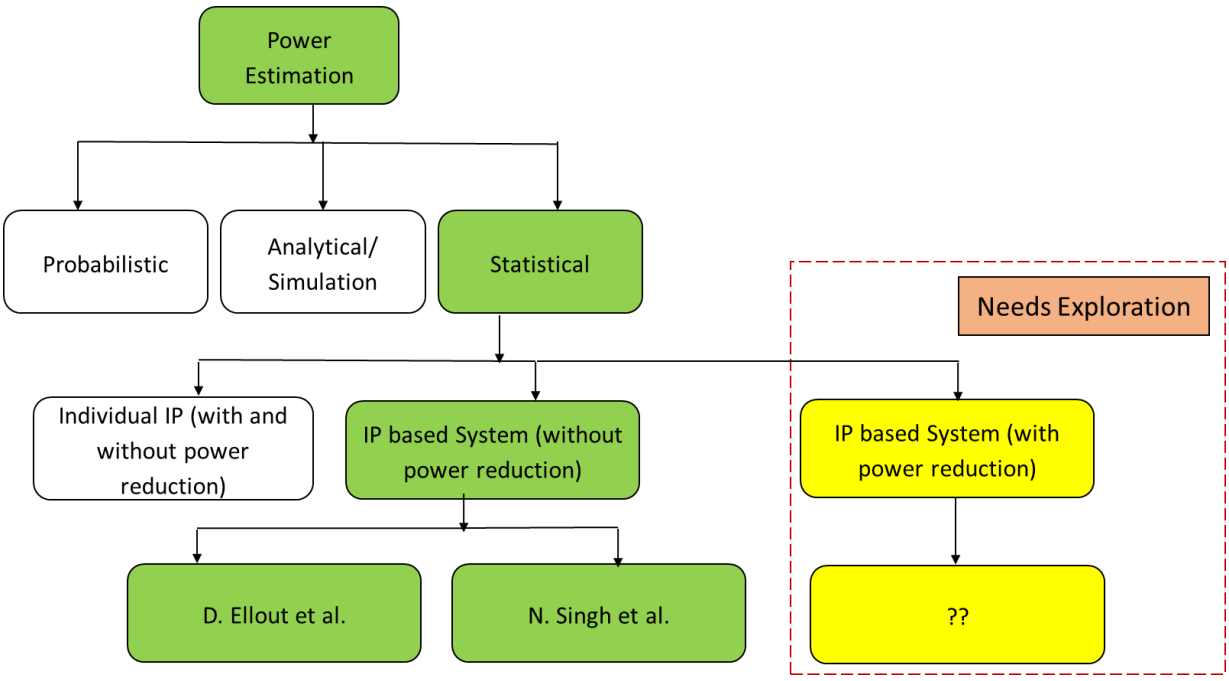

Figure 2. Power Estimation Techniques for FPGAs at Individual IP and System Level.

Conclusions

This work presented an evaluation and analysis of existing FPGA power estimation models with a focus on system-level architectures consisting of multiple IP cores. The study revealed that classical summation of individual IP's power consumption can be used in standard power estimation practices for non-cascaded systems presented where IP blocks are independent. However, significant estimation errors were observed for cascaded systems because switching activity propagates across intermediate IP cores, creating inter-IP dependencies that are not captured by conventional models. The analysis showed that these dependencies can lead to large inaccuracies, particularly in sequential data-flow architectures such as arithmetic and DSP circuits. To address this limitation, a modified power estimation identity was discussed, which reduces the contribution of intermediate IP stages in cascaded architectures, resulting in improved estimation accuracy. The findings emphasize that architectural characteristics must be explicitly considered in system-level power modeling.

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