Performance Investigation of Digital Adders for Vedic Multiplier Design

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Abstract: The performance investigation of various digital adder architectures has been proposed for Vedic multiplier design. In this article, six different adder designs—the Carry Look-Ahead Adder, Han-Carlson Adder, Ripple Carry Adder, Carry Select Adder, Kogge-Stone Adder, Carry Save Adder, as well as a Compressor Adder, are systematically compared with respect to area, dynamic power loss, as well as propagation delay with the Power-Delay Product (PDP). The Cadence design environment is used to implement numerous adder architectures for a 16x16 Urdhva Tiryakbhyam (UT) Vedic multiplier. The synthesis results show that the compressor addition is the most suitable choice to achieve an optimized Urdhva Tiryakbhyam Vedic multiplier. As compared with typical adder architectures, the compressor adder achieved lower hardware area as well as delay. The results of this article are useful to finding out the best and most effective adder topologies for implementing UT Vedic multipliers.

Keywords: Urdhva Tiryakbhyam algorithm; Digital Adders; Hardware area; Cadence design environment; Vedic multiplier; Optimized Power.

Introduction

Multipliers are the most significant and computationally intensive components of digital signal processing (DSP) chains, whose energy and latency profile limits the system's total performance. The main design issues with the current VLSI architecture are minimizing the power dissipation and hardware silicon area and lowering the critical-path delay for the multiplication unit. The sequential dependency that afflicts traditional multiplication methods and results in high latency factors is eliminated by the Urdhva Tiryakbhyam (UT) sutra, also known as the vertically and crosswise method, which enables parallel processing across all the partial products.

Related work

The hardware area of high-speed multiplier design has consistently attracted scientific interest over a number of decades. Ahmed Liacha introduced a windowing booth recoding method to minimize the average amount of additions associated with the single/multiple constant multiplication problem [1]. The architecture successfully integrates collection inside the multipliers' aggregation network by using 5:2 as well as 4:2 compressors using carry save adders and full adders, avoiding inactive cycles and boosting performance [2]-[4]. The XOR-based 4:2 compressor adder was proposed for 8-bit UT Vedic multipliers for image processing applications and was discussed by Dhanasekar et al. [5]. For higher bit

multiplication, computationally efficient compressor adders are consequently required [6]-[8]. Six adder topologies are described in the Table 1 and merged into the 16x16 UT.

Table 1. Comparison of various adders used for 16x16 UT Vedic Multiplier

Adder Type	**Inputs & Outputs**	**Methodology / Working Principle**	**Advantages**	**Area Requirement**	**16x16 UT Vedic multiplier requirement**	**Applications**
Ripple Carry Adder	Inputs: A, B, Cin Outputs: Sum, Cout	Bit-by-bit carry propagation in sequential addition using cascaded full adders	Low hardware requirements and a simple layout	Low	Only appropriate for multipliers with small widths	Low-power embedded systems with simple ALUs
Carry Look-Ahead Adder	Inputs: A, B, Cin Outputs: Sum, Cout	Computes carry in parallel using the Generate (G) and Propagate (P) signals.	Reduced carry delay and faster than RCA	Medium	Suitable for Vedic multipliers operating at medium or high speed	Arithmetic units and DSP processors
Carry Select Adder	Inputs: Cin, A, B Outputs: Cout, Sum	Computes Cin=0 and Cin=1 outputs concurrently and chooses the appropriate result.	Decreased latency in carry propagation	Medium	Ideal for multipliers with moderate speed	Systems for processing signals
Carry Save Adder	Inputs: A, B, Cin Outputs: Sum, Cout	Prevents carry propagation right away; carry is reserved for subsequent stage.	Very fast and excellent for multi-operand addition	High	Excellent for reducing partial products in Vedic multipliers	DSP, MAC units, and Multipliers
Koggle-Stone Adder	Inputs: A, B Outputs: Sum, Cout	Carrys are computed concurrently by a parallel-prefix tree.	High performance and incredibly low latency	Medium	Ideal for 16x16 UT Vedic multipliers	Processor with high performance
Han-Carlson Adder	Inputs: A, B Outputs: Sum, Cout	KSA and Brent-Kung hybrid structures	Optimal trade-off among area and speed	Medium	Effective for Vedic multipliers that are optimized	ASIC, FPGA, and DSP arithmetic modules

Proposed Compressor Adder (4:2)	Inputs: A0–A3, Cin Outputs: Sum, Carry, Cout	Uses XOR, OR, and inverter logic to compress four bits into two outputs.	Reduced area and power, little delay, and effective partial product summation	Low	Suitable for fast 16x16 multipliers	AI accelerators, DSP, and fast speeds multipliers

Key Contribution

The current multiplier topologies need a significant reduction in silicon chip area. In this article, six adder topologies – RCA, CLA, CSLA, CSA, KSA, and 4:2 compressor were discussed. The Cadence Innovus using 45nm semiconductor node was used to implement the adder architectures. The post-synthesis measurements like area, power and delay are extracted using the Cadence Genus tool. A compressor adder design, which also helps for reducing the latency and hardware area in the multiplier design, is used to gather the partial products generated by UT Vedic multiplier.

Method, Experiments and Results

The Compressors will efficiently replace a variety about full adders as well as half adders. which allow them to run at a fast rate. It is called a compressor because it strives to lower the gate count as well as carry latency over the process of adding operations. The proposed adder design completely disregarded the input Cin as well as output Cout compared to the traditional 4-2 adder. By applying a counter characteristic, the 4-2 compressor reduces the four-bit input to produce a two-bit output. The suggested adder lowers the hardware complication by only requiring an OR gate, an XOR, and an inverter. The four-bit input [A1]-[A4] was subsequently XORed up to produce the P_Sum in the 4–2 compressor. By inverting the adjusted P_Sum output while carrying out an OR operation with A4, the P_Carry will be obtained. Partial products obtained through 16-bit Vedic multiplier design were subsequently summed up by suggested 4:2 compressors. A parallel addition for corresponding partial product was speed up the Urdhva Tiryakbhyam multiplication process and reduces needless delay. As a result, the suggested adder lowers the critical latency and increases design efficiency compared to the multiplier design units. When the six adder architectures are implemented as independent 16-bit adder modules, the post-synthesis performance characteristics are summarized in Table 2.

Table 2. Performance Metrics using Six Adder Architectures using 45nm Cadence Genus Tool

Adder Used	Delay (ns)	Power (mW)	Area (μm^2)	PDP (fJ)
RCA	5.78	0.52	312	3.01
CLA	3.12	0.68	485	2.12
CSLA	3.45	0.61	440	2.11
CSA	2.87	0.38	398	1.09
KSA	2.14	0.74	562	1.58
HCA	2.23	0.67	589	1.49
4:2 Compressor	1.82	0.33	321	0.61

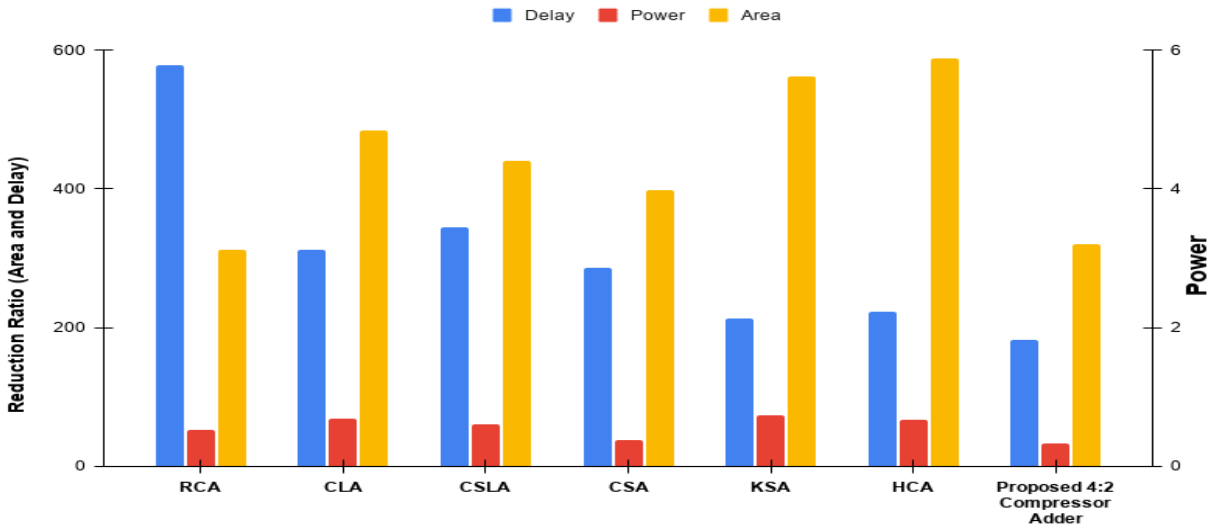

Figure 1. The existing along with proposed 4-2 compressor adders' performance metrics, such as power, delay as well as area

Discussions

Cadence Genus tool having 45nm silicon node was utilized for designing and implementing a performance metrics of different adder topologies, the suggested 4-2 compressor. All adder architectures' performance metrics are shown in Figure 1. The 4:2 Compressor adder's delay is 15.0% fewer versus KSA, 41.7% smaller over CLA, and 68.5% less versus RCA. The 4:2 Compressor Adder attains the lowest dynamic power at 0.33 mW, according to the power consumption measurements. As compared to other adder topologies, the suggested compressor adder attains less area and power, which is best suitable to design a 16-bit UT Vedic Multiplier.

Conclusions

1. In this research article, Cadence Innovus tool with 45nm semiconductor node is employed to a several adder topologies.

2. Based on the Cadence Genus synthesis tool-generated report, an optimized power and hardware area with less latency is obtained in the compressor adder as compared to other adders.
3. In particular, the compressor adder reduces dynamic power by 36% and achieves a 19% less silicon area compared to the HCA adder. These benefits result from the 4:2 compressor adder characteristic, which eliminates carry chain, bottlenecks and permits extremely parallel partial-product reduction because its carry output is independent of its Cin input.
4. The 4:2 compressor-based UT Vedic multiplier offers the greatest energy-delay trade-off presently possible within the analyzed design space for latency-critical applications including real-time DSP, machine learning accelerators, and high-throughput cryptographic engines.

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