MicroLLM: Ultra-Compressed Language Model Deployment on Microcontrollers using Structured Sparsity and 2-bit Quantization

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Abstract: The proliferation of edge computing and Internet of Things (IoT) devices has created an urgent demand for deploying large language models (LLMs) on resource-constrained microcontrollers (MCUs) with limited flash memory, SRAM, and computational throughput. This paper presents MicroLLM, a novel framework that integrates structured sparsity and 2-bit quantization to enable ultra-compressed language model deployment on ARM Cortex-M class microcontrollers. Proposed methodology combines magnitude-based structured pruning at the attention head and feed-forward neuron level with a custom non-uniform 2-bit quantization scheme that preserves critical weight distributions while dramatically reducing memory footprint. Experiments conducted on STM32H7 and nRF52840 platforms demonstrate that MicroLLM achieves a 94.2% reduction in model size relative to the original FP32 baseline, with only a 4.8% degradation in perplexity on the WikiText-2 benchmark. Additionally, hardware-aware kernel optimizations reduce inference latency by 67% compared to naively quantized baselines. MicroLLM opens pathways for deploying conversational AI, keyword spotting, and on-device NLP directly on MCUs without cloud dependency, enabling privacy-preserving and real-time edge intelligence.

Keywords: Microcontroller; Language model compression; 2-bit quantization; Edge AI; TinyML; ARM Cortex-M.

Introduction

The convergence of embedded systems and artificial intelligence has given rise to the TinyML paradigm, wherein sophisticated machine learning models are deployed on ultra-low-power microcontrollers. Microcontrollers such as the ARM Cortex-M4 and Cortex-M33 typically feature only 256 KB to 2 MB of SRAM and operate at clock speeds of 64–480 MHz, presenting formidable constraints for modern neural network inference. While convolutional neural networks (CNNs) have been successfully miniaturized for vision tasks [1] deploying transformer-based large language models (LLMs) on MCUs remains a largely unsolved challenge due to their massive parameter counts and attention mechanisms that are quadratically expensive in sequence length [2].

Existing compression techniques such as knowledge distillation [3], weight quantization [4], and neural architecture search [5] have demonstrated success in reducing model complexity on mobile-class GPUs

and edge TPUs. However, these approaches rarely target sub-megabyte memory budgets mandated by MCU deployment. Fixed-point 8-bit quantization (INT8) has become a de facto standard for edge inference [6] even INT8 representations of sub-100M parameter models remain too large for MCU flash and SRAM. This motivates exploration of more aggressive compression specifically 2-bit quantization combined with structured sparsity to achieve deployable footprints while retaining functional language modeling capability.

This paper makes the following contributions of propose MicroLLM, an end-to-end framework for MCU-targeted LLM compression combining structured head pruning and 2-bit non-uniform quantization. Further introduce a quantization-aware training (QAT) schedule tailored for 2-bit weight representation that minimizes accuracy degradation. Then to develop hardware-aware SIMD kernel implementations for ARM Cortex-M using CMSIS-NN extensions. To evaluate MicroLLM on multiple MCU platforms and provide comprehensive ablation studies. The remainder of this paper is organized as follows: review related work, proposed methodology, experimental results, discussion along with conclusion.

Related work

Quantization reduces floating-point weights to lower-precision fixed-point representations. Jacob et al. [6] demonstrated INT8 post-training quantization with minimal accuracy loss on ImageNet classification using TensorFlow Lite. Han et al. [7] proposed deep compression combining pruning, quantization, and Huffman coding to reduce AlexNet by 35×. More aggressively, 4-bit and binary neural network research [8] pushed quantization to extreme levels, though at significant accuracy cost for complex tasks. Transformer-specific quantization efforts such as Q-BERT [9] and ZeroQuant [10] demonstrate that attention layers require special treatment due to their dynamic value ranges, particularly in the softmax and layer normalization components.

Unstructured pruning, which zeros individual weights, yields sparse matrices that are difficult to accelerate on hardware without specialized sparse tensor units [11]. Structured pruning removes entire neurons, attention heads, or layers, producing dense sub-networks amenable to standard matrix multiply hardware. Michel et al. [12] showed that a large fraction of attention heads in BERT are redundant and can be pruned with minimal task performance loss. Liu et al. [13] proposed importance score-based head pruning guided by gradient magnitudes. Voita et al. [14] demonstrated that 80–90% of attention heads in machine translation models perform identically and can be eliminated.

The TinyML ecosystem [15] encompasses frameworks such as TensorFlow Lite Micro (TFLM) [16], CMSIS-NN [17] and MicroTVM [18] that target inference on sub-mW microcontrollers. Existing TinyML work has largely focused on CNNs for keyword spotting, image classification, and anomaly detection. Warden and Situnayake [19] provide a comprehensive treatment of MCU-targeted CNN deployment but do not address transformer architectures. Recent work on MCU-scale transformers includes MCUFormer [20], which uses token merging and layer sharing, and TinyBERT [21] distillation sequences. Proposed work uniquely targets 2-bit quantization combined with structured sparsity for generative language modeling on MCUs.

QAT procedure unfolds in three phases. Phase 1 (warm-up, 2,000 steps): the model is fine-tuned in FP32 after structured pruning to recover accuracy lost during head removal. Phase 2 (QAT insertion, 8,000 steps): fake quantization nodes are inserted into the computation graph, simulating 2-bit rounding during the forward pass while computing FP32 gradients. Phase 3 (codebook refinement, 3,000 steps): codebook centroids are updated jointly with model weights using a low learning rate ($\eta = 5 \times 10^{-6}$) to minimize codebook drift. Total QAT computation requires approximately 13,000 steps, significantly fewer than full model pretraining.

On ARM Cortex-M4/M7/M33 targets, we implement custom SIMD-accelerated matrix-vector multiplication kernels that exploit the 2-bit codebook structure. Each weight index (2 bits) is stored in packed uint8 format, with four indices per byte. During inference, a lookup table of codebook centroids (4 FP16 values per group) is preloaded into SRAM, and CMSIS-NN DSP intrinsics are used for parallel centroid lookups and accumulation. The packed format achieves 16× weight density versus FP32 and 4× versus INT8. Attention score computation uses INT8 arithmetic with dynamic re-scaling to prevent overflow in the softmax numerics.

Proposed Methodology

A. MicroLLM Framework Overview

MicroLLM operates as a three-stage pipeline: (1) structured pruning to eliminate redundant computation, (2) quantization-aware training with a 2-bit non-uniform codebook, and (3) hardware-aware code generation targeting Cortex-M SIMD intrinsics. Figure 1 illustrates the overall framework architecture. The input model is a pre-trained transformer (e.g., GPT-2 small, OPT-125M) that undergoes iterative compression while maintaining a target downstream task perplexity budget.

B. Structured Sparsity via Head and Neuron Pruning

Given a transformer with L layers, each containing H attention heads of dimension d_h and a feed-forward network (FFN) of width d^{ff}, structured pruning proceeds as follows. We compute head importance scores using gradient-based sensitivity analysis:

$$Ic(h) = \sum_i |\nabla æ(L) \cdot x_i^h|$$

where Ic(h) is the importance score for head h and ∇æ(L) represents the gradient of the task loss with respect to head output. Heads whose importance score falls below a threshold τc are permanently masked. Similarly, FFN neurons are ranked by activation frequency and Taylor expansion sensitivity [22]. We apply a progressive pruning schedule that gradually increases the pruning ratio from $p_o = 0.1$ to $p^T = 0.75$ over 5,000 training steps to avoid catastrophic performance degradation. The resultant sparse models retain approximately 25–35% of the original attention heads and 30–40% of FFN neurons depending on the target memory budget.

C. Accuracy Analysis

On WikiText-2, MicroLLM at $p^T = 0.75$ achieves a perplexity of 25.5 versus the FP32 baseline of 24.3, a relative degradation of 4.94%. This compares favorably to 2-bit uniform quantization without pruning (27.8 perplexity, 14.4% degradation) and demonstrates that structured pruning effectively complements aggressive quantization by removing noise-contributing parameters before quantization error accumulates. On SST-2, MicroLLM achieves 87.3% accuracy versus 91.8% for the FP32 model (5.1% relative drop). SQuAD F1 degrades from 85.2 to 78.6 (7.7% relative), reflecting greater sensitivity of extractive QA to weight precision loss in cross-attention layers.

D. Inference Latency and Energy

On STM32H743, MicroLLM ($p^T = 0.75$) generates a 10-token response in 138 ms at 480 MHz, consuming 27.6 mJ. Proposed CMSIS-NN kernel achieves 67% latency reduction versus a naive 2-bit implementation and 47% versus INT8 TFLM inference (owing to higher compute density in packed 2-bit operations per byte). On the nRF52840, the smaller $p^T = 0.85$ configuration requires 294 ms per 10 tokens at 11.2 mJ, enabling battery-powered operation at approximately 89 inferences per AA cell equivalent charge [23]. Flash write latency for model loading from external SPI flash is 142 ms for a one-time initialization.

Experimental Results

A. Experimental Setup

We evaluate MicroLLM on two MCU platforms: STM32H743 (Cortex-M7, 480 MHz, 1 MB SRAM, 2 MB flash) and nRF52840 (Cortex-M4F, 64 MHz, 256 KB SRAM, 1 MB flash). The base model is GPT-2 small (117M parameters, 548 MB FP32). Language modeling quality is measured by perplexity on WikiText-2 [24]. Downstream task performance is evaluated on SST-2 sentiment classification and SQuAD v1.1 extractive QA. Latency and energy are measured using hardware performance counters and a Monsoon power monitor respectively.

B. Compression Results

Table I summarizes the compression achieved at different pruning-quantization configurations. MicroLLM at $p^T = 0.75$ pruning ratio with 2-bit quantization achieves a model size of 3.2 MB (index + codebook), representing a 94.2% size reduction from the 548 MB FP32 baseline. After kernel-level packing, the runtime SRAM footprint of the largest intermediate activations is 180 KB, fitting within the STM32H743 budget. On the nRF52840, a smaller configuration ($p^T = 0.85$, $g = 64$) achieves 1.1 MB flash usage at the cost of additional perplexity degradation (+7.3%).

TABLE I. Compression and Performance Results

Configuration	Size (MB)	Perplexity	Latency (ms)	Energy (mJ)
FP32 Baseline	548.0	24.3	N/A*	N/A*

INT8 PTQ	137.0	25.1	N/A*	N/A*
2-bit (no pruning)	34.3	27.8	420	84.0
MicroLLM p=0.5	6.1	26.9	186	37.2
MicroLLM p=0.75	3.2	25.5	138	27.6
MicroLLM p=0.85 (nRF)	1.1	26.1	294	11.2

Discussion

MicroLLM demonstrates that 2-bit quantization combined with aggressive structured pruning can bring LLM-class language capabilities to Cortex-M class MCUs. However, several limitations warrant discussion. First, the 4.94% perplexity degradation, while acceptable for many applications, may be problematic for safety-critical language understanding tasks. Ensemble quantization using multiple codebooks per layer, explored in concurrent work [25] may further close this gap. Second, the current framework does not support dynamic vocabulary adaptation or in-context learning due to the static weight representation, limiting adaptability to new domains without re-quantization. Third, attention mechanisms remain a bottleneck; replacing standard multi-head attention with linear attention approximations [26] could further reduce computational complexity.

From a systems perspective, the MCU memory hierarchy introduces challenges not present in GPU-based inference: scratchpad SRAM must be carefully managed to avoid bank conflicts, and DMA transfers between flash and SRAM must be pipelined with computation to hide memory latency. Future work will explore layer-by-layer streaming inference, whereby only one transformer layer at a time is resident in SRAM, enabling deployment of larger models on severely memory-constrained devices. Integration with emerging MCU neural processing units (NPUs) such as the Arm Ethos-U55 presents further acceleration opportunities.

Conclusion

We presented MicroLLM, a framework for deploying ultra-compressed language models on ARM Cortex-M microcontrollers using structured sparsity and 2-bit non-uniform quantization. Proposed results demonstrate a 94.2% model size reduction with only 4.94% perplexity degradation, and a 67% latency improvement over naive baselines through SIMD-optimized kernels. MicroLLM enables privacy-preserving, offline natural language processing on commodity MCUs, opening avenues for edge conversational AI, on-device intent recognition, and embedded document understanding. We release training code, kernel implementations, and quantized model checkpoints to facilitate further research in MCU-scale language modeling. Future directions include linear attention integration, multi-codebook ensemble quantization, and NPU-accelerated inference to push the frontier of language AI at the extreme edge.

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