CORDIC-based Transceiver Architectures for WSN Applications: A Review

Dr. Shashi Raj K[1], Dr. Ajay Kumar[2]

[1]Postdoctoral Researcher, Lincoln University College, Malaysia. Email ID: [1]pdf.shashiraj@lincoln.edu.my

[2]Lincoln University College, Malaysia. Email ID: pdfsv.ajaykumar@lincoln.edu.my

[2]IILM University, Greater Noida, India. Email ID: ajay.phdcse@gmail.com

---

Abstract: Wireless Sensor Networks (WSNs) need low-power, secure, and fast communication methods because sensor nodes have limited energy and computing power. This study examines 25 research publications from the MDPI, IEEE, and Springer databases to showcase current advancements in CORDIC-based digital transceiver topologies for WSN applications. In order to improve communication capabilities and lower computational complexity, the study focuses on hardware-efficient CORDIC algorithmic methods, FPGA-based architectures, and high-throughput transceiver designs. The existing research shows that standardized and pipelined CORDIC topologies significantly reduce latency, power consumption, and device usage. The lack of unified transceiver designs, the restricted integration of lightweight safety procedures, and the inadequate FPGA-level validation under WSN restrictions are some of the remaining drawbacks. Furthermore, there are yet no established benchmarking techniques for comparing performance. The review work highlights that; there is need of secure and integrated CORDIC-based transceiver architecture for future WSN applications.

Keywords: WSN, Transceiver, CORDIC, Review, FPGA

Introduction

The WSNs used to communicate the data among sensors nodes and widely used in many fields like medical field, Environment Tracking system, Industrial robotics, and Construction field. The design of productive interaction hardware continues to be a major problem since these sensor nodes lack adequate power, memory, and computing capabilities [1]. By carrying out modulation, demodulation, timing, and phase-related tasks with the least amount of hardware resources, the digital transceiver significantly contributes to trustworthy communication. The majority of traditional transceiver systems rely on multiplier-driven signal processing methods, which raise processing latency, power usage, and hardware difficulty and restrict their use in low-power WSN contexts [2]. The Coordinate Rotation Digital Computer (CORDIC) method has drawn interest in order to overcome these constraints since it can carry out intricate computations using straightforward shift-and-add calculations. CORDIC-based architectures are appropriate for WSN applications with limited resources since they lower hardware consumption and increase energy efficiency. Nevertheless, latency, efficiency, scaling, and hardware-specific security incorporation remain issues for current CORDIC-based transceiver designs [3–4]. Furthermore, a lot of described designs lack consistent performance analysis under WSN limitations and full FPGA-based system validation. For future-oriented WSN systems, integrable, energy-efficient, robust, and highly efficient CORDIC-based transceiver designs are therefore desperately needed [5].

Method

This study employs an exhaustive review technique to examine current advancements in CORDIC-based designs and WSN-based transceiver systems is shown in Figure 1. Determining the research area was the first step in the study. Next, a systematic literature search was conducted using major scientific databases, such as IEEE Xplore, SpringerLink, MDPI, alongside other indexed journals. According to the Table 1, 429 research publications that were published between 2023 and 2026 were first found. Twenty-five excellent research articles were chosen for in-depth analysis from the 102 papers that were shortlisted following significance screening and open-access filtering. The work uses peer-reviewed articles based on WSN-based Transceivers, CORDIC-based approaches and or on implemented on FPGA/ASIC platforms. The selection process emphasizes on original contribution woks, Hardware-based implementation, and experimental approaches. The approach removes the non-English articles, duplicated papers, survey or review works, unrelated communication works, and non-validated research approaches. The final filtered work is lightweight, more relevant and technical validated list of reference for literature review.

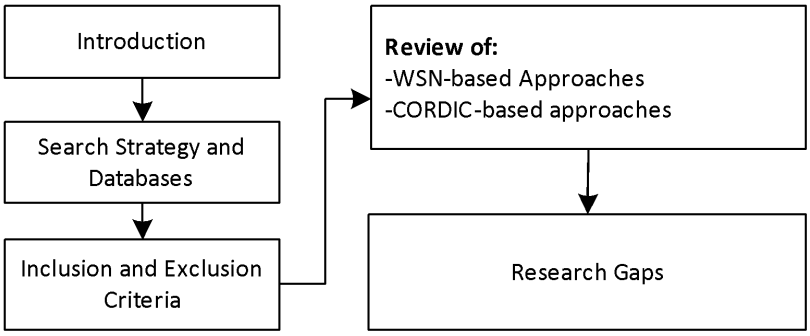

Figure 1. Methodology adopted for review works

Table 1. Databases used in the work

Databases	2023-26	Open Access	Final considered
IEEE Xplore	280	35	11
Springer Link	58	18	7
MDPI	26	26	6
Other Journals	65	23	1
Total	429	102	25

Related Works

WSN-related approaches: This section reviews the existing works of WSN -based transceiver by concerning various approaches, and hardware architectures. Simas et al. [6] describe the GNR-radio based TR framework with the help of LoRa physical layer (PHY) for low-cost, and scalable transmission system. Umezawa et al. [7] present the compact optical WSN model using multi-stacked PIN photodiodes. The work offers 20 Gbps throughput and enhancement in bandwidth of 38-times. Wang et

al. [8] discuss the integrated TX-RX beamforming method for UAV sensing usage which is further used to minimizes the self-interference around 140 dB, with enhancement in tracking accuracy. Chen et al. [9] present the detailed examination of sub-THz transceiver architecture in the D-Band, to solves the design challenges with new optimization approach. Liu et al. [10] describe the CMOS (65-nm)-based D-band transceiver architecture and it offers 200 Gbps, while maintaining the power and noise performance. Yamamoto et al. [11] discuss the full-duplex TR with minimal complexity architecture for IEEE 802.15.4g IoT gadgets. The work obtains the 99 dB self-interference cancellation by employing the hybrid analog-digital methods. Marasinghe et al. [12] proposed a deep learning-based neural TR for improving spectrum efficiency and lowering pilot overhead in phase-noise environments. Haque et al. [13] demonstrated an FPGA-based all-digital aliasing-free PWM transmitter with low EVM that is appropriate for 5G-NR and LTE systems.

CORDIC-based approaches: The existing works of CORDIC-based approaches are discussed in this section Giuffrida et al. [14] introduced TOXOS, a RISC-V compatible coprocessor that can efficiently compute nonlinear and transcendent operations in immediate automotive contexts. Xing et al. [15] proposed a Hybrid Recursive Trigonometric (HRT) technique for FPGA-based frequency synthesizers that eliminates ROM and iterative CORDIC consumption while retaining competitive SFDR and SNR efficiency. Paz & Garrido et al. [16] created an efficient CORDIC-based arcsine/arccosine computing technique with gain correction to decrease approximation error while minimizing hardware complexity. Changela et al. [17] demonstrated a radix-4 hyperbolic CORDIC VLSI design for Nth root and power computing that improves accuracy while reducing hardware use. Nazari and Jamshidi [18] present the Neuromorphic architecture with CORDIC applicability using hardware-based Hindmarsh-Rose neuron model. Bahrami and Nazari [19] discuss the Spatial-Pow-STDP learning method to enhance the Lu, Exp and pow CORDIC units to obtain better accuracy with minimal iterations. Andabili et al. [20] describe the Izhikevich neuron model with CORDIC support to get the 3.18 times higher performance than exiting model on FPGA platform. Zhang et al. [21] present the Optimized CORDIC approach for random-phase digital chirp signal generation and error control mechanism. Paramasivam et al. [22] describe the scaling-free CORDIC architecture using Taylor series approach. This approach minimizes the area, latency and power consumption on FPGA chip. Garrido et al. [23] discuss the uniformly distributed (UD) CORDIC-based architectures are designed to optimize the area, energy and enhance the operating frequency on both FPGA and ASIC platforms. Trivedi et al. [24] present the CORDIC-based SIMD processing element (PE) module with scalable architecture to improve the throughput and accuracy for Deep neural networks (DNN) applications. Luyen et al. [25] describe the approximate-adder design using CORDIC framework for Neuron network works, which offers minimal area, and better energy efficiency.

Research Gaps

The existing works on WSN-based transceivers, CORDIC-based approaches and secured communication approaches are facing many challenges and are listed in this section. Most of the available works focus more on specific features like lightweight security, Throughput enhancement, or CORDIC placement over unified transceiver architecture, which offers better performance metrics like throughput, efficiency, and power all in single platform. This unified feature solves most of the challenges and suitable for WSN deployment. Usage of the suitable optimization approach of CORDIC for WSN application especially in

transmitter and receiver parts. Most of the available architectures do not full use of optimization approaches like iteration reduction, pipelining and optimization of word length, which leads to higher computational hardware complexity and processing time. The available lightweight encryption algorithms are implemented individually and not integrated with transceiver especially for WSN with minimal resource usage. Most of the existing works are simulation-based works and very few are implemented on FPGA platform and its performance comparison. There is a lack of consistent benchmarking comparison under WSN-based transceiver system for Scalability and efficiency parameters.

Conclusion

The CORID -based and WSN-based transceiver architectures with recent advancement are reviewed in this manuscript. The work adopts PRISMA-based methodological approach for systematic review. The work considered year of 2023 to 2026 published papers and selected only 25 suitable and highly relevant articles for review work after filtering. The problem identification, approach, results and limitations are each WSN -based and CORDIC-based works is highlighted in tables. The work also highlights the research gaps from the listed articles. The work highlights the need of unified architecture of digital transceiver with optimal CORDIC approach and lightweight encryption algorithm with hardware validation. Overall, the review work ensures that there is a need of standard unified transceiver architecture which can offers the minimal resource usage, energy, reliability and hardware efficiency for advanced WSN-based transmission system.

References

1. T. Wu, X. Zhou, and W. Fu, “Security issues in software-defined radio: a review,” *Cybersecurity*, vol. 9, no. 1, 2026, doi: 10.1186/s42400-025-00433-x.
2. G. H. Adday, S. K. Subramaniam, Z. A. Zukarnain and N. Samian, "Investigating and Analyzing Simulation Tools of Wireless Sensor Networks: A Comprehensive Survey," in *IEEE Access*, vol. 12, pp. 22938-22977, 2024, doi: 10.1109/ACCESS.2024.3362889.
3. K. Li, H. Fang, Z. Ma, F. Yu, B. Zhang, and Q. Xing, “A low-latency CORDIC algorithm based on pre-rotation and its application on computation of arctangent function,” *Electronics (Basel)*, vol. 13, no. 12, p. 2338, 2024, doi: 10.3390/electronics13122338.
4. N. Thanh Dat *et al.*, “Low-power CORDIC multiplier design using approximate arithmetic for energy-efficient computing,” *vn*, vol. 77, no. 1, pp. 30–42, 2026, doi: 10.47869/tcsj.77.1.3.
5. M. Kim, T. Kim, D. Kwon, and Y. Park, “PUF-based secure authentication protocol for cloud-assisted wireless medical sensor networks,” *Electronics (Basel)*, vol. 15, no. 1, p. 240, 2026, doi: 10.3390/electronics15010240.
6. J. P. de Omena Simas, D. G. Riviello, and R. Garello, “Software-defined Radio implementation of a LoRa transceiver,” *Sensors (Basel)*, vol. 24, no. 15, p. 4825, 2024, doi: 10.3390/s24154825.
7. T. Umezawa *et al*., "Multi-Stacked High-Speed PIN-PD for Compact Mobile Optical-Wireless Transceiver," in *Journal of Lightwave Technology*, vol. 42, no. 11, pp. 4068-4075, 1 June1, 2024, doi: 10.1109/JLT.2024.3378721.
8. L. Wang, X. Li, and Y. Zhang, “Joint transmit and receive beamforming design for a full duplex UAV sensing network,” *Drones*, vol. 9, no. 5, p. 335, 2025, doi: 10.3390/drones9050335.

9. R. Chen, B. Yan, and M.-C. F. Chang, “A review of circuits and systems for advanced sub-THz transceivers in wireless communication,” *Electronics (Basel)*, vol. 14, no. 5, p. 861, 2025, doi: 10.3390/electronics14050861.
10. C. Liu *et al*., "A 640-Gb/s 4 × 4-MIMO D-Band CMOS Transceiver Chipset," in *IEEE Journal of Solid-State Circuits*, vol. 60, no. 4, pp. 1132-1149, April 2025, doi: 10.1109/JSSC.2024.3515640.
11. K. Yamamoto, K. Komatsu, Y. Miyaji and H. Uehara, "In-Band Full-Duplex Transceiver With Low-IF and Shared-LO Architecture for Small IoT Devices," in *IEEE Wireless Communications Letters*, vol. 14, no. 3, pp. 671-675, March 2025, doi: 10.1109/LWC.2024.3519712.
12. D. Marasinghe, L. H. Nguyen, N. Rajatheva and M. Latva-Aho, "Phase Noise Resilient Neural Transceivers for High Data-Rate Sub-THz Links," in *IEEE Wireless Communications Letters*, vol. 14, no. 3, pp. 836-840, March 2025, doi: 10.1109/LWC.2024.3524722.
13. M. F. U. Haque, H. Ahmed, and T. Johansson, “All-digital aliasing-free PWM transmitter with reduced filtering requirements,” *Sci. Rep.*, vol. 16, no. 1, 2026, doi: 10.1038/s41598-026-44436-1.
14. L. Giuffrida, G. Masera, and M. Martina, “TOXOS: Spinning up nonlinearity in on-vehicle inference with a RISC-V CORDIC coprocessor,” *Technologies (Basel)*, vol. 13, no. 10, p. 479, 2025, doi: 10.3390/technologies13100479.
15. X. Xing, W. Melek, and W. Wang, “A Hybrid Recursive Trigonometric technique for direct digital frequency synthesizer,” *Electronics (Basel)*, vol. 14, no. 15, p. 3027, 2025, doi: 10.3390/electronics14153027.
16. P. Paz and M. Garrido, "CORDIC-Based Computation of Arcsine and Arccosine Functions on FPGA," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 9, pp. 3684-3688, Sept. 2023, doi: 10.1109/TCSII.2023.3262353.
17. A. Changela, Y. Kumar, M. Woźniak, J. Shafi, and M. F. Ijaz, “Radix-4 CORDIC algorithm based low-latency and hardware efficient VLSI architecture for Nth root and Nth power computations,” *Sci. Rep.*, vol. 13, no. 1, p. 20918, 2023, doi: 10.1038/s41598-023-47890-3.
18. S. Nazari and S. Jamshidi, “Efficient digital design of the nonlinear behavior of Hindmarsh-Rose neuron model in large-scale neural population,” *Sci. Rep.*, vol. 14, no. 1, p. 3833, 2024, doi: 10.1038/s41598-024-54525-8.
19. M. K. Bahrami and S. Nazari, “Digital design of a spatial-pow-STDP learning block with high accuracy utilizing pow CORDIC for large-scale image classifier spatiotemporal SNN,” *Sci. Rep.*, vol. 14, no. 1, p. 3388, 2024, doi: 10.1038/s41598-024-54043-7.
20. M. N. Andabili, S. Nazari, and T. Moosazadeh, “Chaotic dynamics analysis and digital hardware design of the Izhikevich neuron model,” *Sci. Rep.*, vol. 15, no. 1, p. 16766, 2025, doi: 10.1038/s41598-025-01876-5.
21. H. Zhang, M. Chen, S. Wan, Z. Jiao, S. Hu and P. Song, "An Arbitrary-Phase-Varying Digital Chirp Signal Generator Based on Improved CORDIC Algorithm and Trajectory Approximator," in *IEEE Access*, vol. 12, pp. 135362-135371, 2024, doi: 10.1109/ACCESS.2024.3456554.
22. C. Paramasivam *et al*., "Enhanced Performance of New Scaling-Free CORDIC for Memory-Based Fast Fourier Transform Architecture," in *IEEE Access*, vol. 13, pp. 19828-19844, 2025, doi: 10.1109/ACCESS.2025.3530684.
23. M. Garrido, D. Medina, P. Paz and M. López-Vallejo, "Uniformly Distributed CORDIC," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 72, no. 11, pp. 6948-6961, Nov. 2025, doi: 10.1109/TCSI.2025.3560802.
24. V. Trivedi, G. Raut, B. Mohammad, S. K. Vishvakarma and A. Kumar, "C-SIMD: CORDIC-Driven SIMD Processing Element for Resource-Efficient Multi-Precision Deep Learning Inference," in *IEEE Access*, doi: 10.1109/ACCESS.2026.3653253.
25. V. V. Luyen *et al*., "Energy-Efficient Izhikevich Neuron Design Using Approximate CORDIC-Based Multipliers for Low-Power Neuromorphic Hardware," in *IEEE Access*, vol. 14, pp. 22146-22161, 2026, doi: 10.1109/ACCESS.2026.3662681.