Recent Advances in Quantum Dot Cellular Automata: A Comprehensive Survey

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Abstract: As the Complementary Metal-oxide Semiconductor Technology reaches its physical limitations, classical computing technologies face issues in terms of area, cell count, power consumption, and latency, making it difficult to design high speed, and energy efficient systems. Among the emerging nano-scale technologies Quantum-dot cellular Automata(QCA) is the prominent candidate for future applications. Through the deployment of electron positions within quantum cells, QCA reduces power consumption by enabling binary logic without the need for electric current flow. This paper offers a thorough analysis of QCA technology, focusing on several circuit designs and approaches that have been put out recently. It also discusses the performance parameters of digital circuits like Full adder, Multiplexer, Code Converter and Comparators proposed in various recent articles.

Keywords: Polarization, majority gate, QCA cell, QCA wire, clocking scheme.

Introduction

In the early days, the integration of transistors on a chip followed Moore's law. Today, due to the physical limitations, the secondary effects will dominate in the case of CMOS. The urge to design ultra-low power circuits reaches into the newly evolved beyond CMOS technology called QCA. QCA is a transistor less computing paradigm with an operating speed of THz and a device density of 1012 devices/cm^2. FET-based logic is replaced by the QCA device paradigm, which makes use of the quantum effects of nano scale [1].

QCA Cell

In contrast to CMOS technology's current switching, QCA encodes binary data according to each electron's location. Each cell in the QCA array is made up of quantum dots, which are also thought of as sites that are placed at the square cell's corners. The dots contain the localized charge. Two mobile electrons that can tunnel between the dots make up the cell as well. Due to coulombic repulsion, two free electrons are always found diagonally in the corners of the cells. The four cell structures are common. Hence, two binary states are obtained with a cell, P = -1 indicating logic 0 and P = +1 to refer to logic 1. This enabled the design of digital circuits having two levels of computing logic. Figure 1 displays the four-dot QCA cell with the polarization [2].

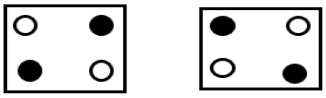

Figure 1. Cell Polarization

QCA Wire

An array of QCA cells constitute QCA wire. The wire transmits input cell state to the output. There are two types of cells called 90 degrees (normal cells) and 45 degrees (rotating cells).

QGA Gates.

The basic QCA gates are inverter and majority gate. The inverter depicted in Figure 2. operates by inverting the electron alignment caused by coulombic repulsion at the corner cell. When electrons have the same polarization as the input cell, they will experience maximal repulsion and instability, causing them to anti-align with it. This is one of the fundamental designs of the inverter, and the corner cell is aligned at 45 degrees relative to the other cells. While alternative designs have been proposed by academics, this one is widely applicable to most circuits.

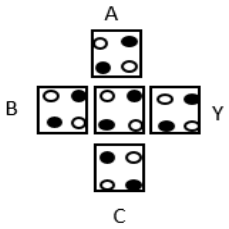

Figure 2. Majority gates

The majority gate is also a crucial gate in QCA. This gate determines the value of the output cell based on the polarization of the majority of inputs, creating a ground state for the device cell (central cell). The majority gate uses the equation (1).

$$Y = AB + BC + AC \quad (1)$$

where A, B, and C are the inputs. The majority gate may build AND and OR gates by applying fixed polarization to one of its inputs. When the input polarization is set to 1, the majority voter works as an OR gate; when set to -1, the gate acts as an AND gate.

QCA Clocking

The clocking in QCA comprises two functions. One is for the synchronization of data flow and the other is to act as an alternative to the power supply as in the case of classical circuits. Clocking primarily controls the tunneling barriers between quantum dots, thereby regulating electron transfer. The QCA clocking scheme comprises four phases: switch, hold, release, and relax. In QCA, cells begin with low potential barriers and no polarization. During the switch phase, surrounding cell polarization pushes a cell into a different state. The tunnel barriers are then lifted, securing this situation. During the hold phase, the cell

retains its polarization and pushes neighboring cells. During the release and relax phases, barriers are reduced, electrons tunnel, and the cell returns to null polarization. The clock zones are color-coded as shown in Figure 3. (zones 0: green, 1: magenta, 2: blue, and 3: white).

Figure 3. Clocking Scheme

Related Work

The digital circuits using CMOS transistors are replaced by QCA technology for improving the performance parameters. Researchers are designing new optimized logic blocks for future application. The main circuits like full adder, multiplexer, code converter and comparator are discussed in this section.

Full adder

The basic unit of a multibit adder is a QCA-based FA. Seyedi, et al have explored a multilayer adder with 18 cells with an area of 0.02 um^2 and a latency of 2 clock cycles [3]. A reversible full adder with 48 cells with area of 0.04um^2 and latency of 2 clock cycles were proposed by Jaiswal [4]. Zohaib, et. al suggested a full adder with 38 cells occupying an area of 0.035um^2 with a latency of 3 clock zones [5].

Multiplexer

In S Kassa [6], introduced another 2:1 multiplexer design consuming 23 cells, 0.04 um^2 area, and 0.5 clock cycle latency. In [7] an optimal, single-layered, 1:2 demultiplexer circuit is proposed using 19 QCA cells with a latency of a single clock cycle. Aswathy et.al explored a demux design with cell count as 15 , occupying an area of 0.02 μm^2 with a latency of 0.5 clock cycles[8].

Code converter

Safaiezadeh et. al in [9] has proposed a novel QCA circuit to convert the 4-bit BtoG code. This conversion method is useful to reduce the rapid switching activity. The BtoG converter is simulated using a suggested XOR structure. This structure is 0.02 μm^2 in size and contains 29 cells. For it to produce the right outputs, two clock zones are required. There is no crossover in this structure. Rezhi in [10] investigated converters based on the tile-based architecture of the QCA XOR gate. In comparison to their equivalent counterparts, the proposed design was implemented with a cell count of 35 and having latency of 0.5.

Comparator

Bahrepour investigated a comparator utilizing two five-input majority gates and one three-input majority gate with 43 cells, 0.08 um^2 area, and five clock cycles delay [11]. A comparator presenting a modular

XOR/XNOR structure consuming 0.04 um^2 area, and 0.75 clock cycles latency is designed in [12] using 47 cells. An optimized comparator was proposed by Shiri et al. [13] by exploring Improved Gate Diffusion Input (IGDI) design specifically for QCA technology as a universal gate. The design occupies 38 cells with 0.03 um^2 area and two clock cycles. Aswathy et al. [14] have introduced two comparator designs, and the best cost-effective co-planar design has 35 cells occupying an area of 0.04 um^2.

Result and Discussion

The comparison of various circuits is listed in table 1. The various performance parameters are area, cell count and latency.

Table 1. Comparison of various QCA circuits

Design	Reference	Area	Cell count	Latency
Full adder	[3]	0.02	18	2
	[4]	0.04	48	2
	[5]	0.035	38	3
Multiplexer	[6]	0.04	23	0.5
	[7]	-	19	1
	[8]	0.02	15	0.5
Code converter	[9]	0.02	20	0.5
	[10]	-	35	0.5
Comparator	[11]	0.08	43	5
	[12]	0.04	47	0.75
	[13]	0.03	38	2
	[14]	0.04	35	0.5

Conclusions

Future applications will concentrate on nanoscale devices as CMOS technology approaches its physical limit; new computer paradigms like QCA are quite promising. This article focuses on the analysis of different modules that are necessary for different applications. Recent circuits such as full adder, multiplexer, code converter, and comparator are compared in terms of cell count, area, and latency. More efficient circuits are needed for upcoming applications including communication and the Internet of Things.

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