Low Power Estimation Framework at System Level for FPGAs

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Abstract: Field Programmable Gate Arrays (FPGAs) are widely adopted in designing high performance and low power embedded systems. However, the power estimation at the system level remains a difficult problem, especially in the case of multiple IP cores. The system-level power estimation models for cascaded and non-cascaded architectures are available in literature. However, the available models are only experimented on conventional designs of moderate and high complexity level circuits that does not incorporate any low power technique. The battery-operated mobile systems need low power designs in order to reduce the battery life. Therefore, this paper presents some power reduction techniques at RTL level and an integrated frameworks that combine IP-level modeling, system-level scalability, and runtime power optimization techniques. The results provide guidance towards accurate and scalable FPGA power estimation approaches for complex heterogeneous systems targeted to low power designs.

Keywords: FPGA; Power Estimation; IP Modeling; IP Cores; Low Power Design

Introduction

Field Programmable Gate Arrays (FPGAs) are the choice of designers for the development of high-performance systems. With the advent of Artificial Intelligence, nowadays FPGAs also find their applications in edge computing, autonomous driving cars, and telecommunications. However, FPGAs suffers from high power consumption. Commercial power analysis and estimation tools are available but due their long design cycles lots of time has been wasted. Therefore, there is a need of early power estimation frameworks. The system-level power estimation models for cascaded and non-cascaded architectures are available in literature. However, N. Singh et. al. modified estimation identity, which takes into account the effect of intermediate IP cores in cascaded architectures. However, this modified identity has not been tested for the designs incorporated with power reduction techniques using the IP modeling approach at system level [1]. Similarly, the conventional IP-summation models proposed by D. Elleouet et. al. can achieve acceptable accuracy for non-cascaded systems but incur large estimation errors for cascaded systems as a result of the propagation of switching activity between IP cores [6].

Literature Review

The literature survey shown in table 1, combines research related to power reduction techniques, power estimation methodology and frameworks. It has been observed from the literature survey that there is no integrated framework available for power estimation that combine IP-level modeling, system-level scalability, and runtime power optimization techniques.

Theme / Category	Core Sub-Technique	Citations	Core Contribution / Methodology
Related to Power Reduction Techniques (Actuators)	**Clock Gating Architectures**	Huda et al. [11] Shinde et al. [12] Wang et al. [16]	Focuses on inserting clock enables and routing-level clock buffers specifically modified for FPGA fabrics (e.g., Virtex-5) to freeze idle logic blocks.
	Fine-Grained RTL & HLS Gating	Li et al. [20], [21] Riahi et al. [24]	Introduces toggle-rate monitoring and centralized/fine-grained clock gating generation directly during High-Level Synthesis loops.
	Memory & Architectural Optimization	Tessier et al. [15] Kumar et al. [13] Verma et al. [18]	Explores algorithms for low-power RAM mapping within embedded BRAM blocks and thermal-aware image ALU configurations.
Related to Power Estimation Methodology (Analytical Models)	**High-Level IP Macro-Modeling**	Liu et al. [5] Elleouet et al. [6] Durrani et al. [8] Gupta et al. [27]	Builds high-level black-box and gray-box functional equations to characterize Intellectual Property (IP) blocks without requiring full physical implementation.
	Switching Activity & Software Estimation	Nasser et al. [9] Lee et al. [17] Lebreton et al. [23] Gebotys et al. [24]	Tracks statistical switching activity propagation across logic networks; includes SystemC Transaction-Level Modeling (TLM) for DVFS and embedded DSP software activity traces.
Related to Accuracy, ML, & Validation Frameworks	**Machine Learning & GNN Forecasting**	Poovannan et al. [2] Lin et al. [3]	Utilizes modern pre-synthesis ML regressions and Graph Neural Networks (PowerGear) on HLS intermediate graphs to bypass tedious CAD implementation times.
	Hardware Measurement & Custom Tools	Lee et al. [4] Verma et al. [10] Davis et al. [22] Anderson et al. [25]	Delivers high-accuracy online, per-module runtime power tracking (KAPow) and cycle-accurate hardware measurements to calibrate analytical tools.
	Commercial Flow Baseline References	Lorandel et al. [7] Chalbi et al. [14] Vivado Guide [19]	Evaluates end-to-end framework accuracy using gold-standard vendor tools (Xilinx Vivado Power Analyzer / UG907) as a base accuracy validation vector.

Table 1. Research related to Power Estimation Frameworks and Power Reduction Techniques for FPGAs.

Power Reduction Techniques at Register Transfer Level

The designers at RTL level have very limited opportunities to reduce the power consumption as shown in figure 1. As power is highly dependent on switching activity, reducing it during the designing process

would greatly impact on power consumption. In clock gating, the switching activity can be reduced by disabling the clock to the unused blocks. Choosing the right FSM encoding reduce toggling and inserting pipelining registers help in reducing glitching. Choosing optimized BRAM blocks over LUTS also reduce switching activity. At system level, unused IPs can be disabled in order to reduce the power.

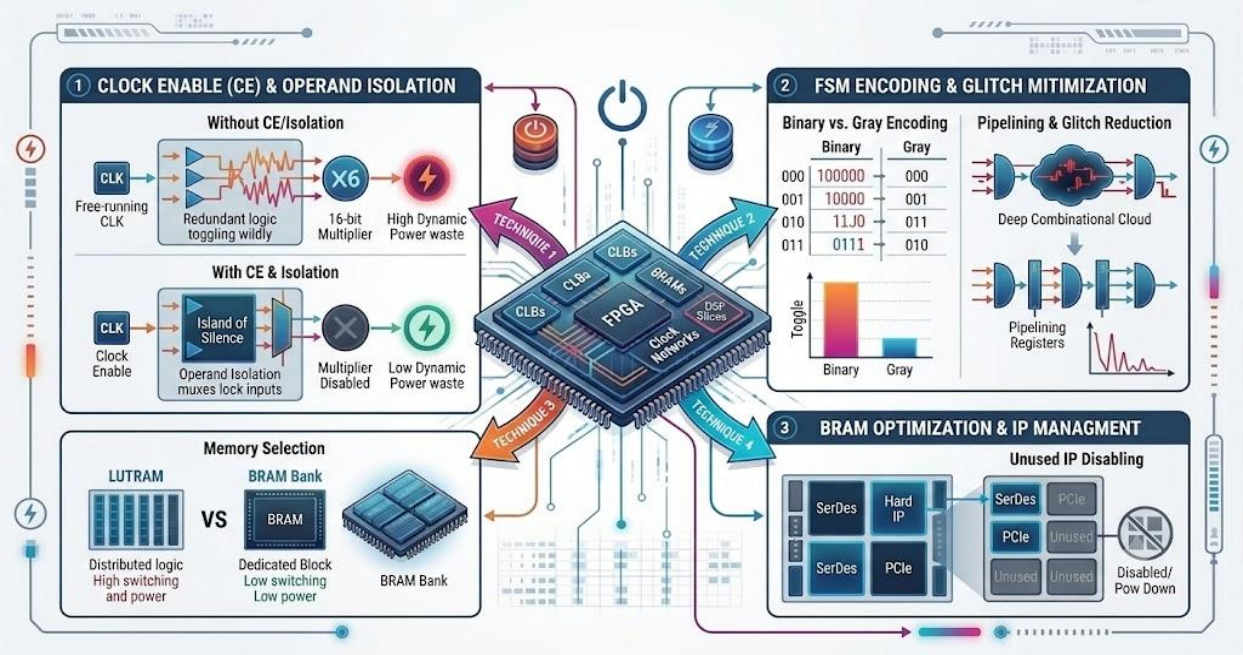

Figure 1. RTL Power Reduction Techniques for FPGAs.

Proposed Methodology

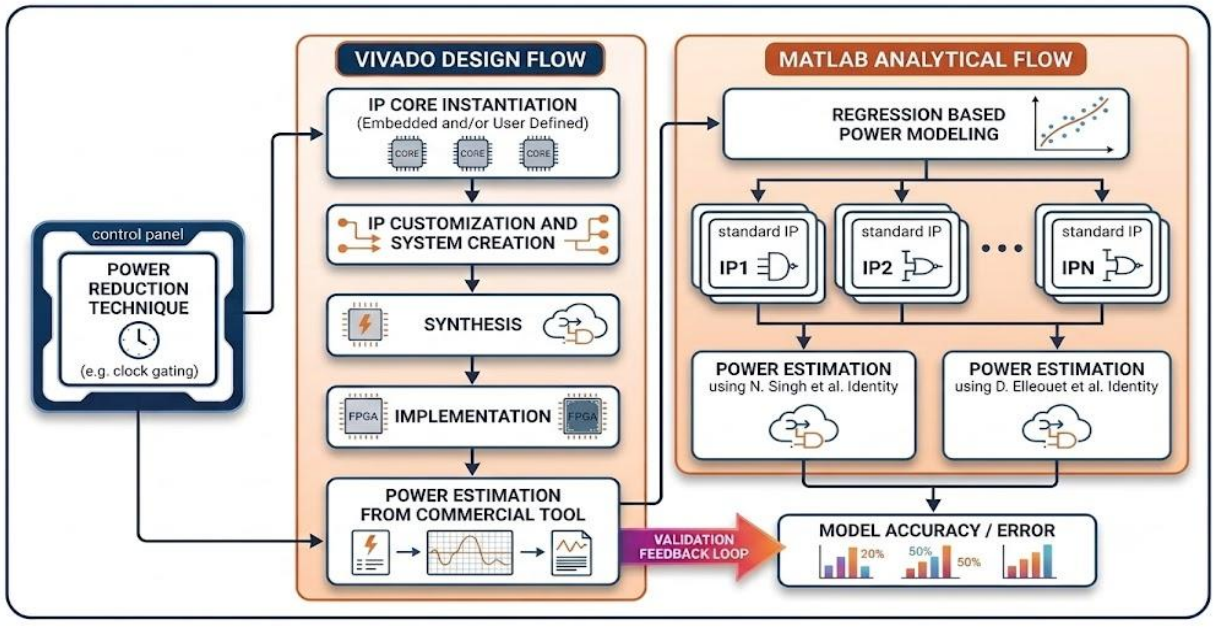

Figure 2. Proposed Low Power Estimation Framework at System Level for FPGAs

The framework of power estimation at system level for low power designs is shown in figure 2. The system level designing requires different IPs (standard or user defined) connected together and customized in order to create a specific system. Each IP is configured with power reduction technique. The system is synthesized and the power is estimated using VIVADO power analysis tool. Later on, each IP is also customized for different input/output vector length and parameterized equations are created using the synthesis data in MATLAB environment. The curve fitting and nonlinear regression technique is generally utilized for obtaining the relationship between dependent and independent variables. Further, the power has been estimated using the approaches given in the literature and compared against the commercial tool for validation purpose.

Conclusion

This work presented a low power estimation framework for FPGAs with a focus on system-level architectures consisting of multiple IP cores. The study revealed that classical summation of individual IP's power consumption can be used in standard power estimation practices for non-cascaded and cascaded systems where IP blocks are independent. This proposed framework can used to evaluate these IP based non-cascaded and cascaded systems.

References

1. N. Singh, G. Verma, V. Khare, “Accurate Power Estimation Identity for DSP Blocks Targeted to FPGAs”, Ingénierie des Systèmes d’Information , vol. 27, no. 4, pp. 539-548, 2022, **doi: 10.18280/isi.270403.**
2. E. Poovannan and S. Karthik, "Pre-Synthesis and Post-Synthesis Power Estimation of VLSI Circuits Using Machine Learning Approach," *Applied Artificial Intelligence*, vol. 36, pp. 3656-3669, 2022, **doi: 10.1080/08839514.2022.2145640.**
3. Z. Lin, Z. Yuan, J. Zhao, W. Zhang, H. Wang, and Y. Tian, "PowerGear: Early-Stage Power Estimation in FPGA HLS via Heterogeneous Edge-Centric GNNs," in *Proc. Design, Automation and Test in Europe Conf. and Exhibition,* pp. 1341-1346, 2022, **doi: 10.23919/DATE54114.2022.9774682.**
4. H. G. Lee, K. Lee, and Y. Choi, "Cycle-Accurate Energy Measurement and Characterization of FPGAs," *Analog Integrated Circuits and Signal Processing*, vol. 42, pp. 239-251, 2005, **doi: 10.1007/s10470-005-6758-5**.
5. X. Liu and M. C. Papaefthymiou, "HyPE: Hybrid Power Estimation for IP-Based Systems-on-Chip," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 24, no. 7, pp. 1089-1103, 2005, **doi: 10.1109/TCAD.2005.850891.**
6. D. Elleouet, N. Julien, and D. Houzet, "A High-Level SoC Power Estimation Based on IP Modeling," in *Proc. IEEE Int. Parallel and Distributed Processing Symp. (IPDPS)*, pp. 1-4, 2006, **doi: 10.1109/IPDPS.2006.1639468.**
7. J. Lorandel, J. C. Prevotet, and M. Helard, "Fast Power and Performance Evaluation of FPGA-Based Wireless Communication Systems," *IEEE Access*, vol. 4, pp. 2005-2018, 2016, **doi: 10.1109/ACCESS.2016.2559781.**
8. Y. A. Durrani and T. R. Alcaide, "High-Level Power Analysis for Intellectual Property-Based Digital Systems," *Circuits, Systems, and Signal Processing*, vol. 33, no. 4, pp. 1035-1051, 2014, **doi: 10.1007/s00034-013-9692-2.**

9. Y. Nasser, J.-C. Prevotet, M. Helard, and J. Lorandel, "Dynamic Power Estimation Based on Switching Activity Propagation," in *Proc. 27th Int. Conf. Field-Programmable Logic and Applications (FPL)*, pp. 1-2, 2017, **doi: 10.23919/FPL.2017.8056783.**
10. G. Verma, V. Khare, and M. Kumar, "More Precise FPGA Power Estimation and Validation Tool (FPEV_Tool) for Low Power Applications," *Wireless Personal Communications*, vol. 106, pp. 2237-2246, 2019, **doi: 10.1007/s11277-018-5938-4.**
11. S. Huda, M. Mallick, and J. H. Anderson, "Clock Gating Architectures for FPGA Power Reduction," in *Proc. IEEE Int. Conf. Field Programmable Logic and Applications (FPL)*, 2009, pp. 112-118, **doi: 10.1109/FPL.2009.5272538.**
12. J. Shinde and S. S. Salankar, "Clock Gating—A Power Optimizing Technique for VLSI Circuits," in *Proc. Annu. IEEE India Conf. (INDICON)*, pp. 1-4, 2011, **doi: 10.1109/INDCON.2011.6139440**.
13. T. Kumar, B. Pandey, S. H. A. Musavi, and N. Zaman, "CTHS-Based Energy Efficient Thermal Aware Image ALU Design on FPGA," *Wireless Personal Communications*, vol. 85, pp. 671-696, 2015, **doi: 10.1007/s11277-015-2801-8.**
14. N. Chalbi, M. Boubaker, and B. M. Hedi, "Accurate Dynamic Power Model for FPGA-Based Implementations," *IJCSI Int. J. Comput. Sci. Issues*, vol. 9, no. 2, pp. 84-89, 2012.
15. R. Tessier, V. Betz, D. Neto, A. Egier, and T. Gopalsamy, "Power-Efficient RAM Mapping Algorithms for FPGA Embedded Memory Blocks," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 26, pp. 278-290, 2007, **doi: 10.1109/TCAD.2006.887924.**
16. Q. Wang, S. Gupta, and J. Anderson, "Clock Power Reduction for Virtex-5 FPGAs," in *Proc. ACM/SIGDA Int. Symp. Field-Programmable Gate Arrays (FPGA)*, pp. 13-22, 2009, **doi: 10.1145/1508128.1508132.**
17. M. T. Lee, V. Tiwari, S. Malik, and M. Fujita, "Power Analysis and Minimization Techniques for Embedded DSP Software," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 5, pp. 123-135, 1997, **doi: 10.1109/92.555992.**
18. G. Verma, M. Kumar, and V. Khare, "Low Power Techniques for Digital System Design," *Indian Journal of Science and Technology*, vol. 8, pp. 1-6, 2015, **doi: 10.17485/ijst/2015/v8i17/75364.**
19. AMD Xilinx, *Vivado Design Suite User Guide: Power Analysis and Optimization (UG907)*, 2022.
20. L. Li, K. Choi, and H. Nan, "Activity-Driven Fine-Grained Clock Gating and Run-Time Power Gating Integration," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 21, no. 8, pp. 1540-1544, 2013, **doi: 10.1109/TVLSI.2012.2212732.**
21. L. Li, K. Choi, S. Park, and M. K. Chung, "Novel RTL-Level Methodology for Low Power Using Wasting Toggle Rate-Based Clock Gating," in *Proc. Int. SoC Design Conf. (ISOCC)*, pp. 484-487, 2009, **doi: 10.1109/SOCDC.2009.5423918.**
22. J. J. Davis, E. Hung, J. M. Levine, E. A. Stott, and P. Y. K. Cheung, "KAPow: High-Accuracy, Low-Overhead Online Per-Module Power Estimation for FPGA Designs," *ACM Trans. Reconfigurable Technology and Systems*, vol. 11, pp. 1-22, 2018, **doi: 10.1145/3129789.**
23. H. Lebreton and P. Vivet, "Power Modeling in SystemC at Transaction Level: Application to a DVFS Architecture," in *Proc. IEEE Comput. Soc. Annu. Symp. VLSI (ISVLSI)*, pp. 463-466, 2008, **doi: 10.1109/ISVLSI.2008.71.**

24. M. Riahi, M. E. Alam, S. Nasab, and S. M. Fakhraie, "Power Efficient High-Level Synthesis by Centralized and Fine-Grained Clock Gating," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 34, no. 12, pp. 1954-1963, Dec. 2015, **doi: 10.1109/TCAD.2015.2445734.**
25. J. H. Anderson and F. N. Najm, "Power Estimation Techniques for FPGAs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 10, pp. 1015-1027, Oct. 2004, **doi: 10.1109/TVLSI.2004.831478.**
26. C. H. Gebotys and R. J. Gebotys, "Statistically Based Prediction of Power Dissipation for Complex Embedded DSP Processors," *Microprocessors and Microsystems*, vol. 23, pp. 135-144, 1999, **doi: 10.1016/S0141-9331(99)00030-7.**
27. S. Gupta and F. N. Najm, "Power Modeling for High-Level Power Estimation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 8, no. 1, pp. 18-29, 2000, **doi: 10.1109/92.820758.**